Stitching a Reference Plane Split Using Routing Layer Traces to Improve I/O Bus Signal Integrity

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Abstract— While on-board interconnects are operating at much higher frequencies, the cost of the overall computing system has been decreasing. Computer manufacturers are therefore continuously looking for ways to lower the production cost. In a mobile computing system, where size is a main constraint and expensive high layer count printed circuit board (PCB) technology has been used to control routing congestion, using cheaper technologies with a smaller number of routing layers is an attractive mean of controlling manufacturing cost. On the other hand, routing on a severely size-constrained mobile platform with a smaller number of routing layers can inadvertently expose wide high speed digital interfaces to non-ideal conditions such as reference plane gaps produced by various power and ground islands. Multi-GHz operation of these high speed signals also means that the traditional mitigation method of adding bypass capacitors across the reference gaps is becoming ineffective. In this paper, we propose to use stitching patch underneath the splitting power and ground plane that can be used in conjunction with bypass capacitors to mitigate the effect of these reference plane gaps on signal quality, as well as system EMI and ESD.

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1. INTRODUCTION

In the past few decades, microprocessor operating frequency has increased from a few megahertz to multi gigahertz. Board-level high speed digital interfaces, such as system bus, system memory, and system I/O, that carry information between microprocessor, memory controller, I/O controller, and other components, however, have been operating at a lower frequency. This is in part because transmission line and other higher order electromagnetic effects can dominate board-level interconnect designs due to electrically significant interconnect sizes. Yet, due to the ever increasing demand for more bandwidth, operating frequencies of these board-level high speed interfaces have also been doubling in roughly two-year cycles. Parallel high speed interfaces such as Front-Side Bus (FSB) and Double Data Rate-III (DDR-3) SDRAM, for example, are fast approaching 1 GT/s, where significant frequency content can extend well into multi-GHz. In the mean time, PCI Express-like serial differential high speed interfaces, already operating at speeds over 1 GT/s, are designed into new cross-chip interconnects such as the Direct Media Interface (DMI). Routing a system with such a large number of high speed digital buses while insuring signal integrity, EMI compatibility, and ESD susceptibility, is a challenge.

The power and ground planes are generally used as reference planes for high speed I/O buses. As the number of power supply rails increased dramatically in desktop and mobile systems, multiple power planes on a real estate constraint platform often forces high speed interfaces to cross different reference planes. It is a known fact that when high speed transmission lines cross a reference plan split, cross coupling and radiated emission are greatly increased [1–5]. Increased cross coupling leads to greater-than-expected signal quality degradation, and on critical interfaces, have been known to cause signaling failures. Added radiated emission, on the other hand, may lead to system Electromagnetic Interference (EMI) failure. We have known cases of such EMI failures such as when DDR2 signals crossed a reference plane split and coupling large amounts of common mode noise to nearby LVDS signals, which in turn lead to platform EMI failure.

In most cases when reference plane crossing is unavoidable, discrete decoupling capacitors are used to reduce its impact to signal integrity, as show in Figure 1. However, discrete decoupling capacitors have finite parasitic inductance, making them less effectiveness at high frequencies. Typical on-board decoupling capacitors have a resonance frequency on the order of a few hundreds Mega Hertz (MHz). On the other hand, however, typical high speed interfaces have frequency contents greater than 1 GHz. Discrete capacitors also add to board cost.

In this paper, we "stitch" a reference plane split below with a conductor patch on the second routing layer, and use the parasitic capacitance between the patch and the second reference plane to reduce the effect of reference plane crossing.

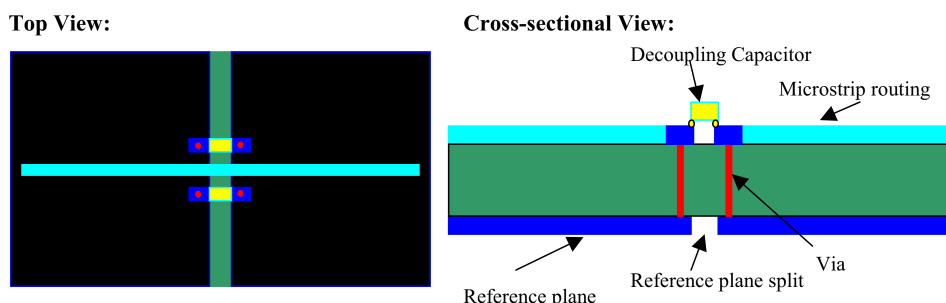
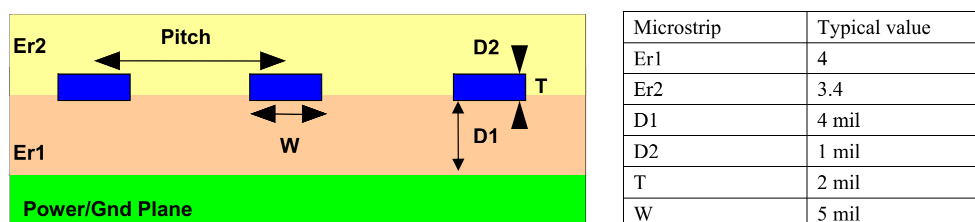


Figure 1: Decoupling capacitors are used to reduce the effect of crossing a reference plane split.

2. REFERENCE PLANE DISCONTINUITY STUDY

We studied the microstrip line performance due to the reference plan gap based on the typical microstrip geometries on computer mother board as shown in Figure 2. All microstrip transmission line study in this paper is based on the geometries descript in Figure 2 with 5000 mil length.



Microstrip	Typical value
Er1	4
Er2	3.4
D1	4 mil
D2	1 mil
T	2 mil
W	5 mil

Figure 2: Typical microstrip transmission line geometry for computer mother board.

Interconnects over a split power/ground plane are evaluated using 3D EM simulator HFSS. Based on the HFSS simulation, we observed the E-field discontinuity when the reference plane has slot or complete gap as shown in Figure 3. The splitting reference plane effects to interconnect transmission performance were plotted in Figure 4 with various gap widthes comparing with ideal transmission line.

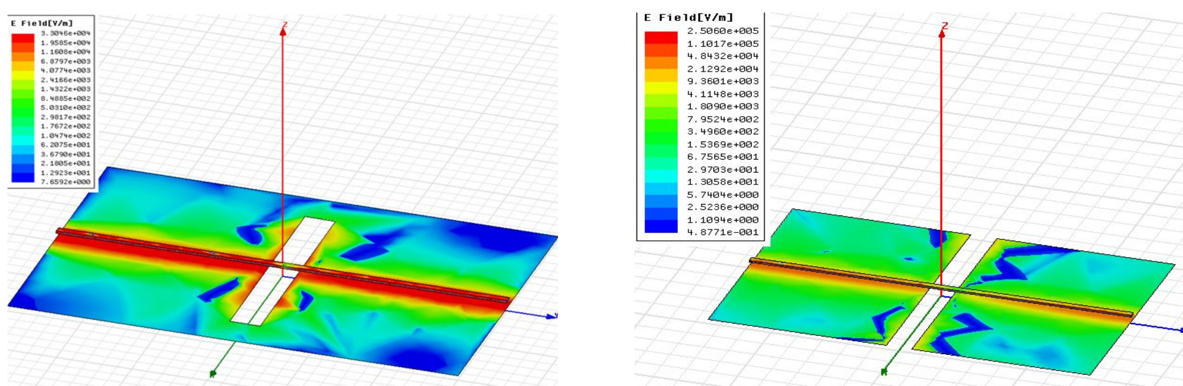


Figure 3: E-field distribution plot for reference plane slot (left) and complete split (right).

From the Figure 4, we observed that the gaps in reference planes cause discontinuities on microstrip lines to increase transmission loss as frequency goes up. Splitting reference plane causes more severe transmission line performance degradation comparing with slot opening in reference plane. As the width of the slot/split increase, the trace transmission loss increase further.

3. MITIGATION METHOD FOR SPLITTING REFERENCE PLANE

Our approach to solve splitting reference planes is to stitch a conductor patch on the second routing layer below the reference plane split, as show in Figure 5. Here we use vias to connect the patch

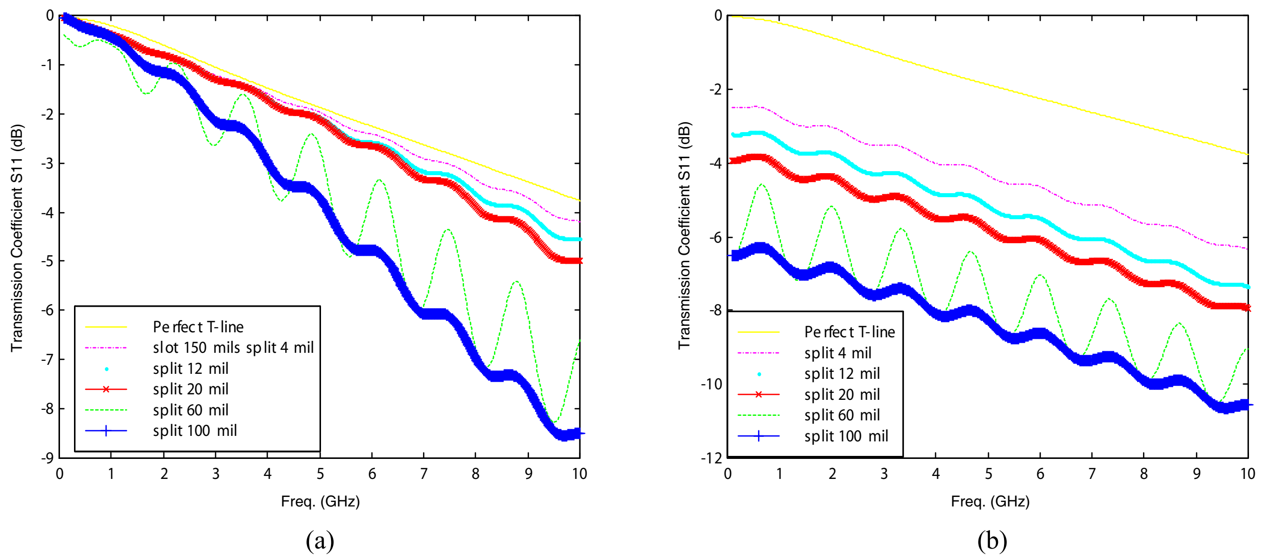


Figure 4: Microstrip line transmission coefficient with different split gap width 4, 12, 20, 60, 100 mil for 150 mil long slot gap on reference plane (left) and complete reference plane split (right).

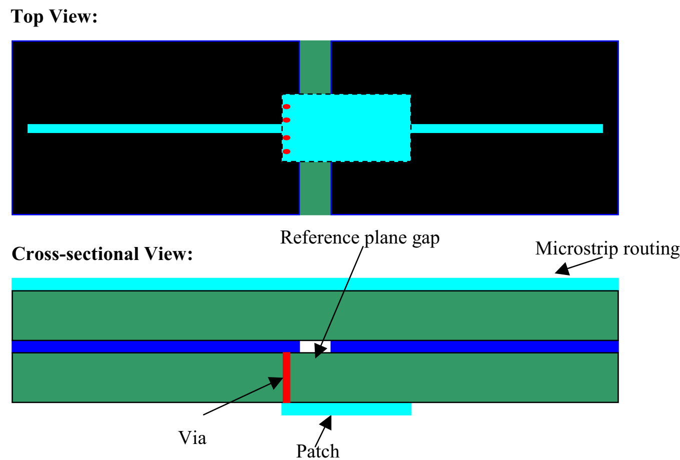


Figure 5: A patch on the routing layer below the reference plane is used to reduce the effect of reference plane split.

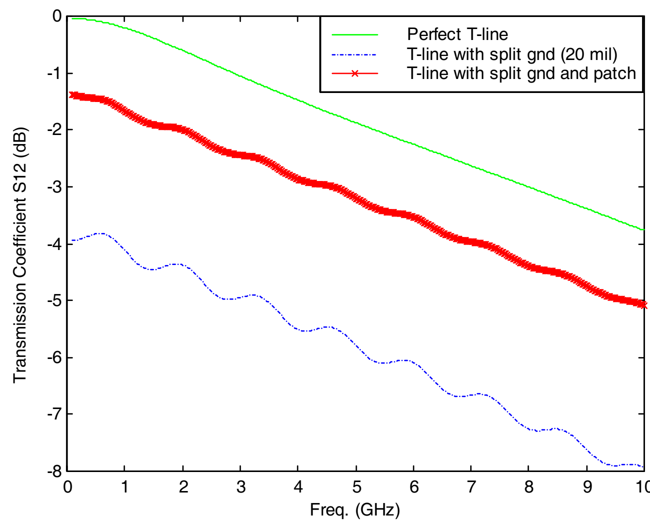


Figure 6: Input reflection coefficient comparison of perfect T-line, T-line with split ground (20 mil gap) and patch (40 mil wide and center via) with split ground T-line.

to one reference plane and use parasitic capacitance between the patch and the second reference plane to reduce the effect of reference plane crossing. Using the parasitic capacitance between two parallel plates (patch and the second reference plane) allows a continuous return path beneath the high speed I/O signal that must cross the reference plane split. The transmission loss plot in Figure 6 is shown the conducting patch beneath the splitting reference plane reduce reference plane split effects by ∼3 dB. Compare to the prior art of using discrete decoupling capacitors to provide a return path, this approach is much more effective at high frequencies and is more cost effective.

The main advantage of using a conductor patch on the routing layer below the reference plane to reduce the effect of reference plane split is its effectiveness at high frequencies. Past its self resonance frequency, a discrete decoupling capacitor is no long effective. Given most of the high speed I/O signals have significant frequency content in Giga-Hertz range, using decoupling capacitors is not an effective mean to reduce the impact of reference plane splits. The conductor patch, on the other hand, is effective for frequencies up to 100 GHz. The BOM cost is also reduced because discrete components are not needed.

4. CONCLUSION

Impact of reference plane split to transmission line performance was presented in this paper. A stitching conducting patch beneath splitting power/ground plane to reduce the reference plane split discontinuities effect was proposed. Based on the HFSS simulation results, we observed stitching conducting patch effectively reduce the reference plan split effects.

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