A UHF RFID Reader Receiver SoC in 0.18 μm CMOS Technology

C. C. Zhang[1,2], Y. Q. Qian[1,2], J. Zhao[1,2], Y. Zhang[1,2], D. B. Wang[1,2], and Y. F. Guo[1,2]

[1]Jiangsu Provincial Engineering Laboratory of RF Integration and Micro-assembly
Nanjing University of Posts and Telecommunications, Nanjing 210023, China
[2]College of Electronics Science & Engineering
Nanjing University of Posts and Telecommunications, Nanjing 210023, China

Abstract— A fully-integrated single-chip receiver for an 860–960 MHz UHF RFID reader is designed in 0.18 μm CMOS technology. It is mainly composed of an RF front-end, a DC offset cancellation (DCOC) block, and an analogue baseband. The RF front-end consists of a double-mode low noise amplifier (LNA) and an I/Q mixer. The LNA can operate under two different modes, which correspond to the listen-before-talk (LBT) mode and the normal mode specified by UHF RFID protocols, respectively. The common-gate structure and the dynamic current injection technique are used for the mixer to achieve high linearity and low 1/f noise. The analogue baseband comprises a programmable gain amplifier (PGA) and a low-pass filter (LPF). The opamp-based PGA is composed of a fine gain stage with a gain step of 1 dB, and a coarse gain stage with three fixed gain, corresponding to 6 dB, 12 dB and 24 dB, respectively. The LPF is a fourth-order Butterworth active RC one, whose bandwidth can be adjusted between 480 kHz and 1.68 MHz. Simulation results show that the receiver achieves $P_{1\,\mathrm{dB}}$ of −2.1 dB in LBT mode and sensitivity of −88 dBm in normal mode, with power dissipation of 95.72 mW from a 1.8 V power supply.

1. INTRODUCTION

Radio frequency identification (RFID) techniques have found rapidly-growing applications in many areas, such as supply chain managements and object tracking systems, which present diverse and demanding needs for application-specific and sophisticated design techniques [1]. The direct-conversion architecture along with standard CMOS technologies is widely preferred for RF readers among various solutions because of the reducing cost and improving integration level [2]. As for a UHF RFID system, one of the most challenging issues within the reader receiver design is to make a proper tradeoff between linearity and noise figure [3].

In this paper, a fully-integrated 860∼960 MHz CMOS RFID reader receiver system on a chip (SoC) is presented in 0.18 μm CMOS technology. The simulated $P_{1\,\mathrm{dB}}$ is −2.1 dB in the listen-before-talk (LBT) mode, and the simulated sensitivity is −88 dBm in normal mode. Compared with the previous works in standard 0.18 μm CMOS technology [1–3], this receiver shows high linearity with similar gain and power consumption.

2. RECEIVER ARCHITECTURE

The highly-integrated direct-conversion receiver architecture is employed for the RFID reader receiver, shown in Fig. 1. The receiver consists mainly of an RF front-end, an analogue baseband, and a DC offset cancellation (DCOC) bock. The RF front-end comprises a low noise amplifier (LNA) and a I/Q down-conversion mixer. The analog baseband is composed of baseband programmable gain amplifiers (PGA), and low pass filters (LPF). Due to its many advantages over a single-ended one, the fully-differential topology is applied here.

The LNA is designed specifically to improve sensitivity in the listen-before-talk (LBT) mode, and in the meanwhile, to achieve high linearity in the normal mode. And then, the amplified RF signal is fed into the I/Q mixer, by which it is demodulated to produce two I/Q baseband signals. The local I/Q clocks are generated by an external frequency synthesizer.

Owing to the diversified application environments, the amplitude of the RF signal coming to the antenna before the receiver varies largely. The PGA is aimed to amplify adaptively the incoming analog signal to one with a proper amplitude level for the downstream analog-digital converter (ADC). The LPF is used to filter out out-of-band noises to improve the signal-to-noise ratio (SNR) of the signal which will come into the ADC. The LPF is also programmable to accommodate different transmission data rates.

It's well known that the DC offset issue is one of the trickiest issues, which, as for a UHF RFID receiver, becomes more complicated, because both transmitter and receiver operate on a same frequency. In order to overcome the DC offset issue, a DCOC block is inserted between the RF front-end and the analog baseband.

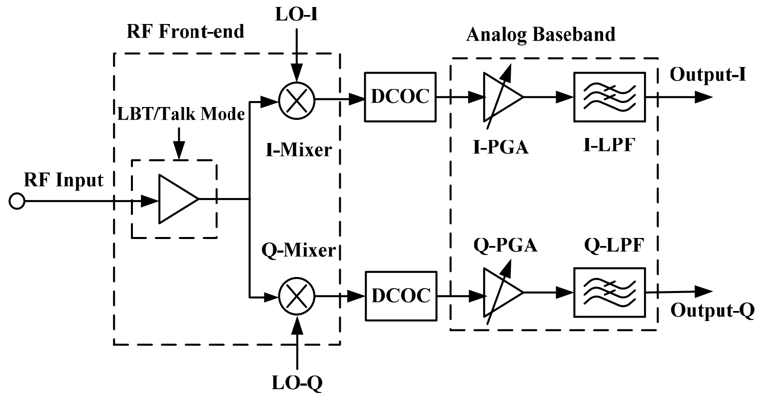

Figure 1: Block diagram of the UHF RFID reader receiver architecture.

3. KEY BUILDING BLOCKS

3.1. Low Noise Amplifier

According to the LNA shown in Fig. 2, by changing the bias voltage Vb2, the MOS transistors M1 and M2 can operate in two different regions. Usually, M1 and M2 operate in saturation region, and then the LNA has higher gain, which is fit for the normal mode. However, if Vb2 is set to a higher voltage, M1 and M2 can operate in triode region, and then the LNA has higher linearity, which is fit for the LBT mode.

The introduction of the coupling capacitors (C3 and C4) will improve both gain and noise performance of the LNA [4]. The tradeoff among impedance matching, gain, noise and linearity is made carefully when the optimization is executed.

3.2. Down-conversion Mixer

Indicated in Fig. 3, the common-gate structure and the dynamic current injection technique are used for the mixer to achieve high linearity and low 1/f noise.

Compared to the traditional Gilbert mixer, the common-gate configuration of input stage (M1-M2) will provide more voltage headroom for the pre-stage driver, and also higher linearity can be obtained for the mixer. The dynamic current injection technique used in the switching stage injects current when nearly all of the transistors are turned on, which can greatly reduce 1/f noise while white noise performance are almost unaffected.

Two mixers shown in Fig. 3 can comprise an I/Q mixer, when two I/Q local clocks are provided for the two mixers, respectively.

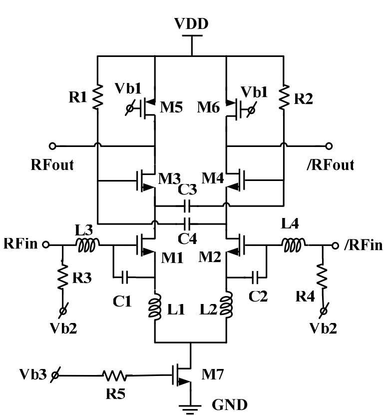

Figure 2: Schematic diagram of the LNA.

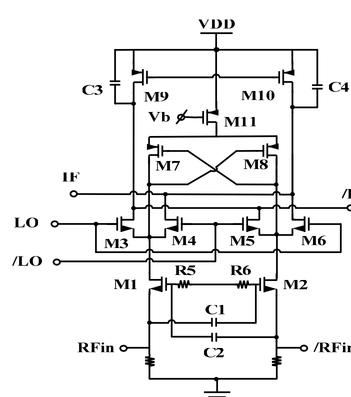

Figure 3: Schematic diagram of the mixer.

3.3. DC Offset Cancellation Block

A DC offset cancellation (DCOC) block, shown in Fig. 4, is applied after the output of the mixer to remove the annoying DC offset. The pre-amplifier has a gain of 10 dB to suppress the noise afterwards.

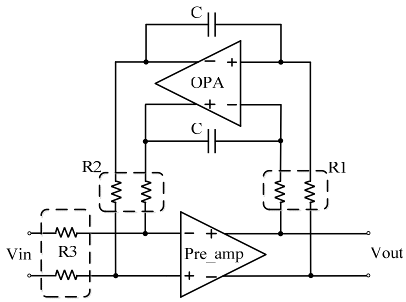

Figure 4: Topology diagram for the DC offset cancellation (DCOC).

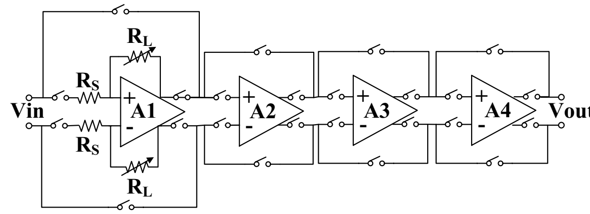

Figure 5: Illustration diagram for the PGA.

3.4. Programmable Gain Amplifier

The PGA is depicted in Fig. 5. The opamp-based PGA is used for good linearity performance. The operational amplifier A1 has a maximum gain of 6 dB, which can tuned in gain step of 1 dB by the resistance ratio of variable resistor arrays R_L and R_S. The fixed-gain amplifiers A2-A4, all adopting the source negative feedback technique to improve their linearity performance, have gains of 24 dB, 12 dB and 6 dB, respectively.

3.5. Programmable Baseband Filter

The baseband low-pass filter is used as a channel selection filter to reject out-of-band interferers and noise. The filter is illustrated in Fig. 6, which is a fourth-order Butterworth active-RC differential one.

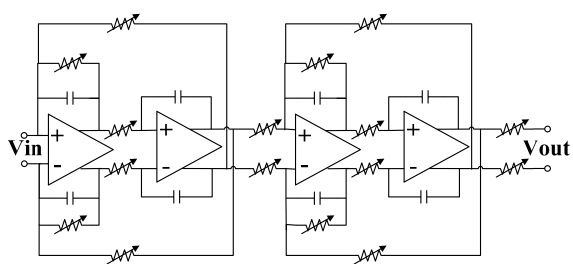

Figure 6: Illustration diagram for the programmable LPF.

In order to meet the channel bandwidth requirements from the UHF RFID direct conversion receiver, the cutoff frequency, that is, the bandwidth of the LPF is adjustable between 480 kHz $\sim$ 1.68 MHz, by controlling the relevant resistor sizes. The design scheme allows the receiver to accommodate a variety of different transmission rates from 40 kb/s to 640 kb/s, and adapt to the LBT mode and normal mode respectively.

4. SIMULATION RESULTS

The simulated $P_{1\,\mathrm{dB}}$ of the proposed RF front-end in the normal mode is shown in Fig. 7 (a). It could be seen from this figure that the $P_{1\,\mathrm{dB}}$ is as high as -2.1 dBm. Fig. 7(b) shows the noise figure characteristic of the LBT mode. The NF characteristic achieves 11.8 dB at 900 MHz.

Figure 8 depicts the measured gain error of the PGA and the channel select characteristics of the LPF. The gain control range is from 0 dB to 48 dB in a step of 3 dB and the maximum gain error is less than 0.9 dB as shown in Fig. 9(a). The frequency response characteristic is shown in Fig. 9(b). The cut-off frequency is 489 kHz, 595 kHz, 696 kHz, 910 kHz, 1.09 MHz, 1.61 MHz adjustable. The out-of-band rejection achieves 50 dB.

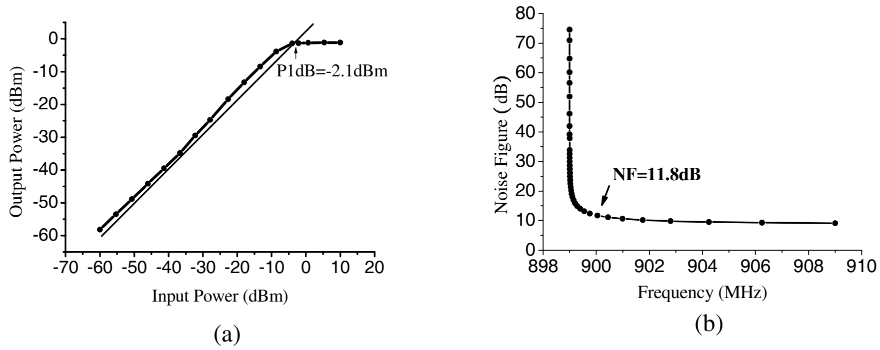

Figure 7: Simulated results of RF front-end (a) $P_{1\,\mathrm{dB}}$ in the normal mode (b) noise figure in the LBT mode.

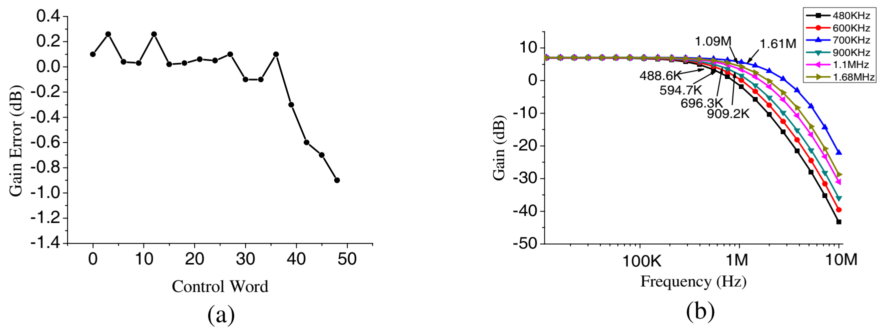

Figure 8: Simulated results of (a) PGA gain error (b) LPF frequency response.

The major chip performance is summarized in Table 1. The sensitivity of the receiver could achieve −88 dBm with the bandwidth of 1 MHz in the normal mode. When working in the LBT mode, the sensitivity of the receiver improves. The comparison between state-of-the-art works and this work is given in Table 2, in which all the works are designed in 0.18 μm CMOS technology.

Table 1: Summary of receiver performance.

Parameters	**Simulated Results**	
	Normal	**LBT**
Operation Frequency	860–960 MHz	
$P_{1\,\mathrm{dB}}$(RF front-end)	−2.1 dB	−9.8 dB
Gain(RF front-end)	3 dB	12 dB
Sensitivity	−77 dBm	−88 dBm
Gain Range	3–51 dB	12–60 dB
Power Consumption	95.72 mW	
Supply Voltage	1.8 V	

Table 2: Comparison with state-of-the-art works.

Parameter		[1]	[2]	[3]	**This Work**
$\mathbf{P_{1\,dB}}$ **(RF front-end)**	**Normal**	3.5 dBm	−8 dBm	7 dBm	−2.1 dB
	LBT	−9.4 dBm	NA	−7 dBm	−9.8 dB
Sensitivity (RF front-end)	**Normal**	−70 dBm	NA	−77 dBm	−77 dBm
	LBT	−90 dBm	−81 dBm	−87 dBm	−88 dBm
Gain Range		10 dB–94 dB	3.6 dB–86.5 dB	NA	3 dB–60 dB
Power Consumption	**Normal**	105.6 mW	135 mW	74 mW	95.72 mW
	LBT			122 mW	

5. CONCLUSIONS

A direct-conversion receiver has been designed for a UHF RFID reader. The double-mode RF front-end achieves high linearity in normal mode and high sensitivity in LBT mode. The bandwidth of the LPF and the gain of PGA are programmable. Simulations of the receiver are done with a standard 0.18 μm CMOS technology in CADENCE.

ACKNOWLEDGMENT

This work was sponsored by the Provincial Natural Science Foundation of Jiangsu (No. BK20130878, BK2012435, BK20141431), the Jiangsu Province Science and Technology Support Program-Industry Part (No. BE2013130), the Specialized Research Fund for the Doctoral Program of Higher Education (No. 20133223120005, 20133223110003), and the Jiangsu Provincial postgraduate scientific research and innovation projects (No. SJLX_0374, SJLX_0375).

REFERENCES

1. Wang, W., S. Lou, K. Chui, et al., "Single-chip UHF RFID reader in 0.18- μm CMOS," *IEEE Custom Integrated Circuits Conference*, 111–114, 2007.
2. Ye, L., H. Liao, F. Song, et al., "A 900 MHz UHF RFID reader transceiver in 0.18 μm CMOS technology," *IEEE 9th International Conference on Solid-State and Integrated-Circuit Technology*, 1569–1572, 2008.
3. Sun, X., B. Chi, C. Zhang, et al., "A 1.8 V 74 mW UHF RFID reader receiver with 18.5 dBm IIP3 and −77 dBm sensitivity in 0.18 μm CMOS," *Radio Frequency Integrated Circuits Symposium*, 597–600, 2010.
4. Koo, K., et al., "Noise figure degradation analysis of power ground noise on 900 MHz LNA for UHF RFID," *IEEE Electronics Packaging Technology Conference*, 416–420, Singapore, 2007.
5. Kwon, I., Y. Eo, H. Bang, et al., "A single-chip CMOS transceiver for UHF mobile RFID reader," *IEEE Journal of Solid-State Circuits*, Vol. 43, No. 3, 729–738, 2008.