

# A CMOS I/Q Up-conversion Mixer and a Power Pre-amplifier for UHF RFID Reader Systems

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**Abstract**— A high gain, high linearity, low noise I/Q up-conversion mixer and a programmable gain power pre-amplifier are designed in a standard 0.18  $\mu\text{m}$  CMOS process, which are both the critical building blocks in a transmitter for UHF RFID reader systems. To comply with the system specifications, both low noise figure (NF) and high LO-IF isolation for the up-conversion mixer are required, so the I/Q mixer topology based on two coupled double-balanced Gilbert cells is applied. Besides, other techniques such as the pseudo-differential structure and the active load are also used to improve its linearity, gain, etc.. As for the power pre-amplifier, a programmable gain fully differential cascode configuration is employed to satisfy the emission spectrum requirements from various application environments. A 3-bit control word is used to switch the three parallel trans-conductance transistors in each side to change the output power flexibly. And the source inductance negative feedback technique is adopted to achieve a good trade-off among noise matching, impedance matching, linearity and gain. From a single 1.8 V power supply, simulation results show that the up-conversion mixer has a total conversion gain of 4 dB, an input 1 dB compression point (IP1 dB) of 4.84 dBm, and an input NF of less than 20.9 dB. The power pre-amplifier has an output 1 dB compression point (OP1 dB) of better than 2.8 dBm, a gain of above 7 dB, and a good input impedance matching.

## 1. INTRODUCTION

UHF radio frequency identification (RFID) is a remote auto-identification technology with many advantages such as a relatively long recognition range, anti-collision characteristics for multi-tag scenarios, a high data rate and a small antenna size [1]. Nowadays, UHF RFID reader is evolving towards miniaturization and low cost with integration in CMOS technology.

For the transmitter of the RFID reader, which is shown in Figure 1, one of the most important building blocks is the up-conversion mixer, which converts the base-band signal to an RF signal mostly based on a double sideband (DSB) up-conversion. In view of this, it should have high linearity and low NF to comply with the specifications of the UHF RFID communication standard [2–5]. Besides, a programmable gain power pre-amplifier (PA) is designed after the mixer to match the reader, which can change the output power of the pre-amplifier flexibly.

Different DC and AC signals can be combined in the quadrature two I/Q circuits of the RF transmitter. In addition, different modulation according to protocol requirements of the system can be achieved through digital baseband filter.

To date, several excellent CMOS up-conversion mixers have been reported [6–8]. For example, in [6], a 1.9 GHz high linearity up-conversion mixer was designed. Though the IP1 dB of 0 dBm is achieved, its 19.8 mW power consumption and 0.35  $\mu\text{m}$  process are not good enough. In [7], a 2.4 GHz up-conversion mixer on wireless sensor networks SoC chip was demonstrated. In spite of

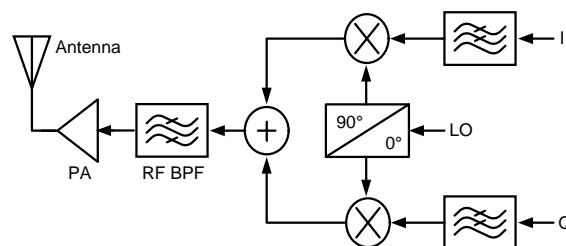


Figure 1: Architecture diagram of the up-conversion transmitter system.



reader systems, the programmable gain fully differential cascode circuit is chosen for the power pre-amplifier. The circuit can be divided into two stages: the common-source amplifier with inductance negative feedback circuit and the common-gate amplifier.

As the circuit is completely symmetrical, any half to be analyzed is enough. As input tubes, M1–M3 are all controlled by a digital circuit, which is connected in parallel. In order to achieve the simultaneous match between input impedance and the noise, circuit uses source inductance LS negative feedback technology. However, if the inductance value is excessive, the CG of the pre-amplifier will be reduced. Therefore, there is a tradeoff between the CG and the circuit match. Then, the input impedance of the half circuit can be expressed as Eq. (3)

$$Z_{\text{in,single}} = s(L_g + L_s) + \frac{1}{sC_{\text{gs}}} + \omega_T L_s \quad (3)$$

M7 as a second stage can reduce the interaction between the input and output terminal of the pre-amplifier as well as the influence of the Miller effect. At the same time, the output terminal uses the off-chip inductor as the load.

In real applications, the distance between the tag and reader is always changing, thence the input terminal use three amplifier input NMOS transistors connected in parallel. When 3 bit digital control switch turned on, the CG of the pre-amplifier can be expressed as Eq. (4)

$$A = (g_{m1} + g_{m2} + g_{m3}) \cdot Q_{\text{in}} \cdot R_{\text{out}} \quad (4)$$

where  $Q_{\text{in}}$  is quality factor of the input resonant network, and  $R_{\text{out}}$  is equivalent output impedance of the pre-amplifier.

### 3. SIMULATION RESULTS

#### 3.1. Up-conversion Mixer

The quadrature up-conversion mixer is designed and simulated in a standard 0.18  $\mu\text{m}$  RF CMOS process. The supply voltage is 1.8 V. Figure 4 shows the CG, IP1 dB, NF and DSB-ASK modulation of the mixer, respectively.

As is seen in Figure 4(a), the amplitude of the mixer is  $-14.01$  dB when the fundamental frequency is 10 MHz. After the conversion, at the center frequency of 910 MHz, the amplitude is  $-10.07$  dB, so the total CG is 4 dB. The power amplifier stage to reduce the difficulty of the design can be seen from Figure 4(b), the IP1 dB of the mixer is 4.84 dBm. That means the circuit has a good linearity. When comes to Figure 4(c), input NF is less than 20.9 dB, while Figure 4(d) shows the DSB-ASK output waveform modulation of the mixer. And Table 1 shows the total simulation results of the proposed mixer.

#### 3.2. Power Pre-amplifier

The power pre-amplifier is also designed in a standard 0.18  $\mu\text{m}$  process and simulated. Figure 5 shows the match characteristic between input and output terminal, transmission characteristic, NF and output linearity of the power amplifier under different conditions of the gain settings, respectively.

As is seen in the figures, the simulation results show that the worst output linearity OP1 dB is better than 2.8 dBm when the power amplifier has a gain of 7 dB, and a match characteristic of  $50 \Omega$ .

Table 1: Simulation results of the mixer.

Parameters	Simulation Results	Units
Operating Voltage	1.80	V
Input IF Frequency	35.452	MHz
Output RF Frequency	150~950	MHz
Consumed Current	29.49 (core current: 7.54)	mA
Conversion Gain	3.94	dB
Noise Figure	20.9	dB
Input P <sub>1dB</sub> point	4.84	dBm

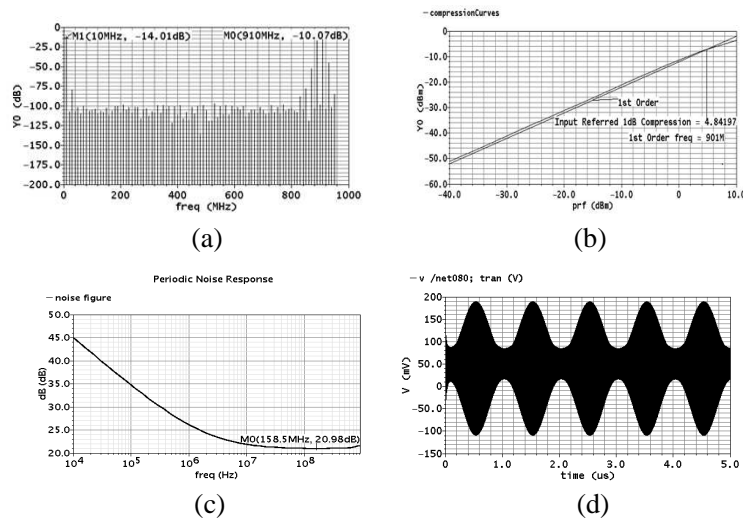


Figure 4: Simulated results of the mixer (a) CG, (b)  $IP_{1\text{dB}}$ , (c) NF, and (d) DSB-ASK modulation.

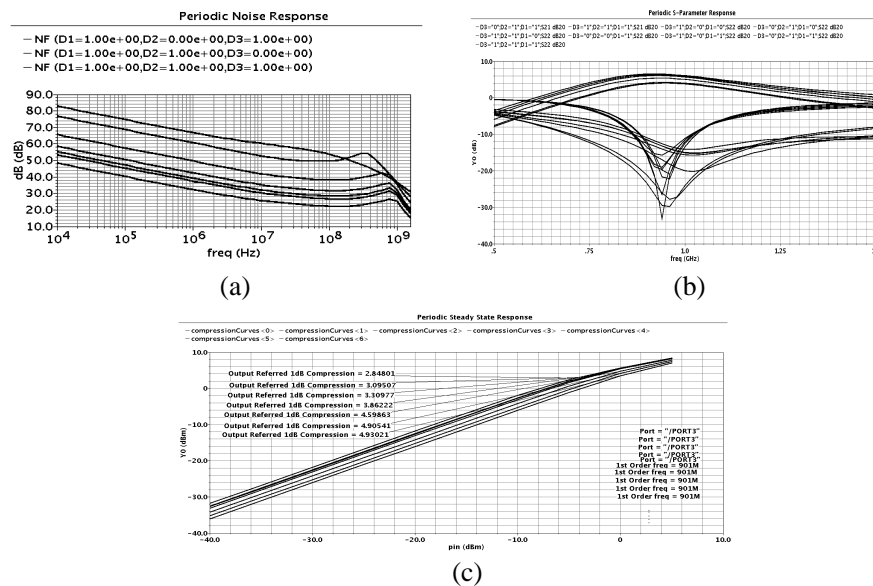


Figure 5: Simulated results of the power pre-amplifier, (a) noise factor, (b) transmission and match characteristics, and (c) output linearity.

#### 4. CONCLUSIONS

A high performance quadrature up-conversion mixer along with a programmable gain power pre-amplifier for the RF front-end transmitter of UHF RFID reader system are designed in  $0.18\ \mu\text{m}$  CMOS process. Considering the stringent requirements of the system, Gilbert double-balanced circuit configuration is picked out for the mixer. In addition, in order to satisfy the emission spectrum of dense and multi-reader system, the programmable gain fully differential cascade circuit configuration is applied to the power pre-amplifier. Simulation results show that they can meet the requirement of the UHF RFID reader system.

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