

Design of Evaluation Board with a Built-in 25 Gb/s PRBS Source for Testing High-frequency Probe

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Abstract— In this paper, an evaluation board with a built-in 25 Gb/s PRBS source was developed for testing high frequency probe (pogo pin) in time domain. The high frequency probes in semiconducting testing field are one of convincing contact elements selections. A commercial clock-data-recovery (CDR) chip was used to design the PRBS source. The 25 Gb/s PRBS signal with 14.2 ps rise time, 15.6 ps fall time, and 14.2 ps time jitter can be generated from our evaluation board. Some printed circuit board (PCB) layout techniques were used to design the 25 Gb/s evaluation board. The advantages of our 25 Gb/s evaluation board for testing high frequency probe have low cost, small size, and light weight.

1. INTRODUCTION

There are more and more internet applications, such as internet TV, multimedia network, online games, social networking sites and cloud computing. We need to decrease the time of the data processing and increase the quality of the data transmission. For higher data rate applications, the 40/100 Gigabit Ethernet standards was proposed in 2010 [1]. The 100GBase can use four parallel 25 Gb/s channels to achieve the transmission rate [2]. Therefore, the performance of the high data rate products, modules, devices, or testing kits need be measured over 25 GHz frequency range.

The time domain measurement of high-speed signal needs generally an expensive pattern generator to provide a pseudo-random binary sequence (PRBS) signal and the volume of the high-speed measurement system is bulky. Therefore, we will design an evaluation board including PRBS source and microcontroller unit (MCU) for reducing the volume, weight, and cost of high-speed measurement system.

Some printed circuit board (PCB) layout techniques were used to design the 25 Gb/s evaluation board. The differential traces were designed to reduce noise interference, and the length of signal traces was short as possible for improving the transmission bandwidth. Using a clock-data-recovery (CDR) chip, our 25 Gb/s PRBS generator was designed. The CDR chip can be controlled by a MCU chip through firmware. The graphical user interface (GUI) software was also developed to conveniently control MCU and read/write data. The communication between the firmware and the software is through the universal serial bus (USB) interface because the USB is a popularity connector between computers and electronic devices. The high frequency probe (pogo pin) is tested through our evaluation board with a built-in 25 Gb/s PRBS source and through a commercial PRBS generator, the results are compared and discussed.

2. DESIGN OF MODULE CIRCUITS

The PRBS generator on our evaluation board used Gennum GN2425 chip, and the circuit diagram is shown in Figure 1(a). The MCU on our evaluation board used Atmel ATmega328P chip, and the circuit diagram is shown in Figure 1(b). The surge protection device IC was also used on our evaluation board to avoid large transient voltage to damage the PRBS generator and the MCU. The π -type filter circuits were also designed on our evaluation board to filter out noise from the power supply.

3. DESIGN OF PCB LAYOUT

On our evaluation board the impedance match of differential trace and single-end trace is taken into account and designed carefully. Under the coupling capacitor, the anti-pad is designed for the impedance match of signal trace [3]. The differential traces were designed to reduce noise interference, and the length of signal traces was short as possible for improving the transmission bandwidth.

Because the high-frequency signal traces are on the top and bottom layers of our PCB, the dielectric material of the top and bottom layers used Rogers 4350B with dielectric constant 3.66. The dielectric material of other layers used FR-4 or Polypropylene (PP), and our evaluation board

is designed as a six-layer PCB. Special K connectors with 40 GHz bandwidth were used in signal input and output interfaces.

Figure 2 shows the PCB layout of the top and bottom layers of our evaluation board. Our evaluation board with a built-in 25 Gb/s PRBS source for testing high frequency probe was fabricated and is shown in Figure 3.

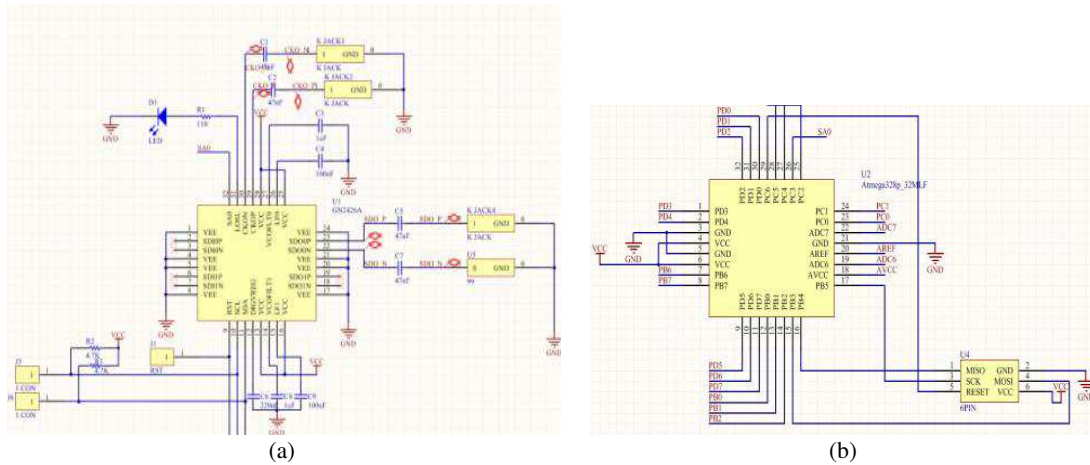


Figure 1: (a) The circuit of PRBS generator (GN2425) and (b) the circuit of MCU (ATmega328P).

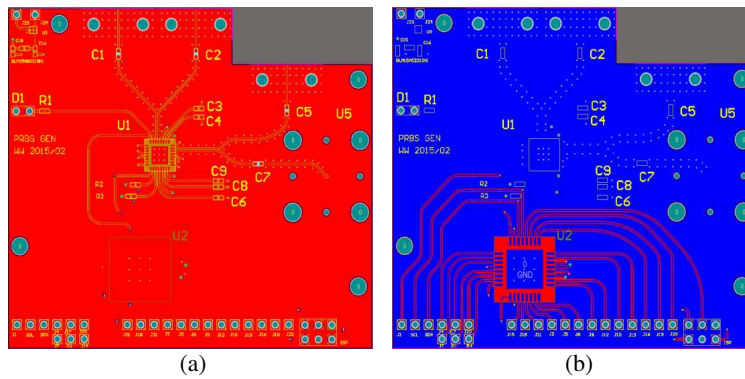


Figure 2: The PCB layout of the (a) top and (b) bottom layers of our evaluation board.

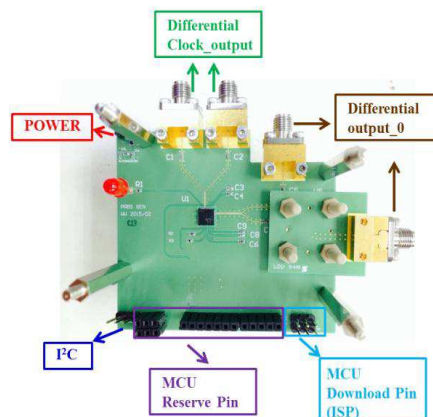


Figure 3: The evaluation board with a built-in 25 Gb/s PRBS source for testing high frequency probe.

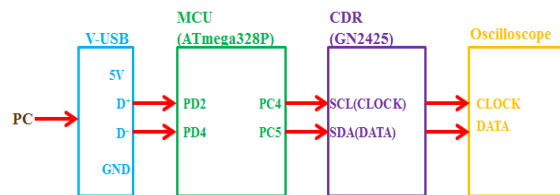


Figure 4: Flow chart from PC command to PRBS signal.

4. DESIGN OF SOFTWARE AND FIRMWARE

The USB is a popularity connector between computers and electronic devices, so the USB is considered to use as an interface between the firmware and the software on our evaluation board. Because the Atmel MCU is used, we used the V-USB [4] to develop USB hardware. The V-USB is a software-only implementation of a low-speed USB device for Atmel AVR MCU, making it possible to build USB hardware with almost any AVR MCU, not requiring any additional chip.

The communication between MCU and GN2425 chip is through I²C (Inter-Integrated Circuit) [5], the I²C is a serial communication bus developed by Philips. I²C uses only two bidirectional open-drain lines, serial data line (SDA) and serial clock line (SCL). I²C provides every devices with 7-bit address but retains 16 addresses, so it can allow 2⁷-16 devices on bus.

Atmel Studio 6 is the integrated development platform for developing and debugging Atmel AVR MCU based applications. Using Atmel Studio 6 the firmware can be burned into the MCU Atmega328P through Atmel's AVRISP mkII burner.

Using computer GUI, the command of personal computer (PC) can be sent to control the MCU through V-USB. The MCU can control the CDR chip to generate PRBS signal through I²C. The PRBS and clock signals can be sent into a digital oscilloscope to measure eye diagram. Figure 4 shows a flow chart from PC command to PRBS signal on our evaluation board.

5. RESULTS OF MEASUREMENT

Figure 5 shows the eye diagrams of 25 Gb/s PRBS signals from our evaluation board and Anristu pulse pattern generator MT1810A. The parameters of 25 Gb/s original eye diagrams are shown in Table 1. The quality of PRBS signal from Anristu pulse pattern generator is better than from our evaluation board, but the quality of our PRBS signal is still desirable

Using our evaluation board and Anristu pulse pattern generator, the performance of high frequency probe (pogo pin) is measured in time domain and the eye diagrams of 25 Gb/s PRBS through the pogo pin is shown in Figure 6. The parameters of 25 Gb/s eye diagrams of pogo pin testing are shown in Table 2. The rise time and fall time of the eye diagram from our evaluation board are similar to from Anristu pulse pattern generator, because the transmission bandwidth is limited by the high frequency pogo pin. Because of the attenuation of the pogo pin, the eye highs of both eye diagrams are attenuated about 42% from our evaluation board and Anristu pulse pattern generator Therefore the 25 Gb/s high frequency probe can be tested through our evaluation board with built-in PRBS source.

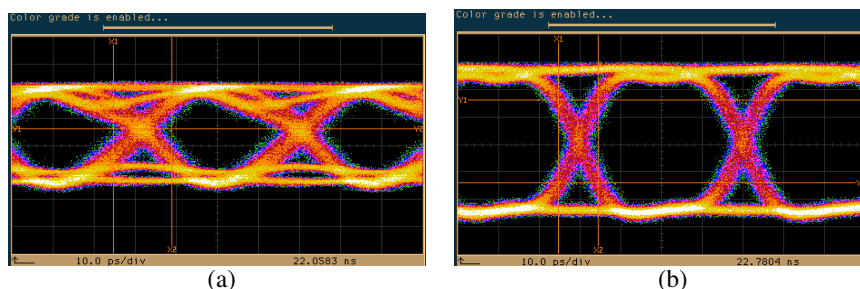


Figure 5: 25 Gb/s original eye diagrams from (a) our evaluation board and (b) Anristu (MT1810A).

Table 1: Parameters of 25 Gb/s original eye diagrams.

	Jitter	Rise time	Fall time	Eye width	Eye high	Q factor
Our evaluation board	14.2 ps	14.2 ps	15.7 ps	24.3 ps	100.4 mV	8.0
Anristu (MT1810A)	9.0 ps	9.5 ps	9.7 ps	31.2 ps	405.8 mV	16.0

Table 2: Parameters of 25 Gb/s eye diagrams of pogo pin testing.

	Jitter	Rise time	Fall time	Eye width	Eye high	Q factor
Our evaluation board	18.7 ps	38.9 ps	51.3 ps	20.2 ps	42.4 mV	4.6
Anristu (MT1810A)	11.1 ps	42.0 ps	40.6 ps	41.1 ps	172.7 mV	5.4

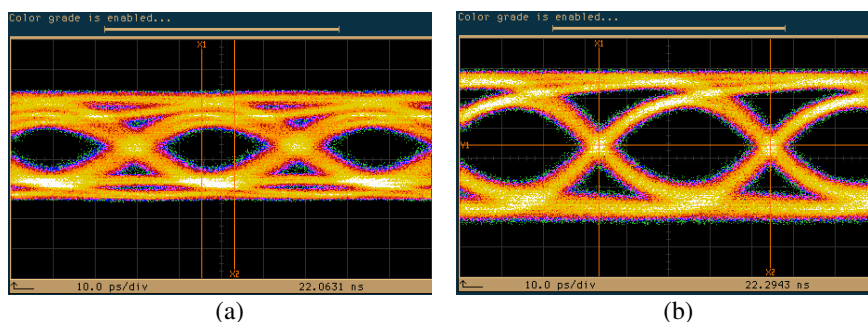


Figure 6: 25 Gb/s eye diagrams of pogo pin testing using (a) our evaluation board and (b) Anristu (MT1810A).

6. CONCLUSION

We have successfully used Gennum GN2425 chip to develop a built-in 25 Gb/s PRBS generator on our evaluation board. Some PCB layout techniques have been used to design the 25 Gb/s evaluation board. The differential traces were designed to reduce noise interference, and the length of signal traces was short as possible for improving the transmission bandwidth. Our evaluation board with a built-in 25 Gb/s PRBS source has been also applied to measure the performance of the high-frequency probe (pogo pin) in time domain. Although the performance of eye diagram from our evaluation board is not as good as from the commercial pulse pattern generator, but the advantages of our evaluation board have low cost, small size and light weight. In the future, we can use a better PRBS generator chip and improve PCB layout to design the better evaluation board, and our evaluation board can also apply to test the other electronic device in high-speed time domain.

ACKNOWLEDGMENT

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