Investigation of a Miniature and High Gain On-chip V Band Microstrip Antenna

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Abstract— This paper presents a miniature and high gain on-chip V band microstrip antenna. A ground plane on the bottom metal layer M_1 has been approached to shield the wave from penetrating into the low-resistivity and high dielectric constant Si substrates to improve the antenna performance. Antenna parameters have been investigated to obtain an optimized antenna with 0.87 mm $*$ 1.16 mm occupation. The measured and simulated return loss results and simulated radiation pattern results of proposed antenna have been presented. The performance of the proposed antenna as compared to other published on-chip antennas has also been demonstrated.

1. INTRODUCTION

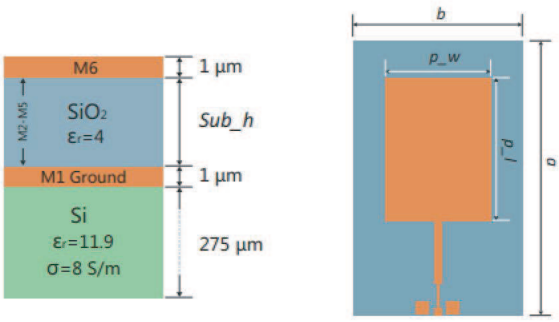
Recently, the increasing demands for high data rate over 100 MB/s wireless communications and compact volume with high performance [1] urge the developments of V band integrated circuits (IC). On-chip-antenna technology brings great chance to reduce the size of Complementary Metal-Oxide Semiconductor circuits (CMOS) for the less work in the impedance match with antenna. However, high dielectric constant, low-resistivity Si material and thin substrate make it difficult to design and fabricate high performance on-chip antenna in standard CMOS technology.

Different kinds of methods have been approached to solve the problem. Some authors [2] tried to solve the problem by adopting a silicon lens at the backside of the chip which changed the standard CMOS technology and cost a lot. Others improved the antenna performance by doing the research of antenna radiation mechanism. Different shapes of antenna such as dipole [3], inverted F [4], yagi [5] and slot [6] has been designed to fit with the circuits. However, the radiation efficiency and the gain still can't achieve a higher level.

In this paper, we approach the total bottom metal layer M_1 to work as a ground plane and shield the wave from penetrating into the low-resistivity and high dielectric constant Si substrates. The energy loss in the Si substrate has been reduced to improve the antenna performance. Considering the great occupation of the patch and thin substrate which is only $\lambda/500$ (around 10 µm), the investigation of patch radiation mechanism has to be done to obtain a miniature and high gain on-chip V band microstrip antenna. The process of design and simulation in the proposed antenna has been done through High Frequency Structure Simulator (HFSS) from Ansoft Corporation based on finite-element-method.

2. ANTENNA DESIGN

Figure 1 shows the geometry of the proposed on-chip patch antenna. This structure consists of a rectangular patch antenna on the top metal layer M_6 and a ground plane on the bottom metal layer M_1. In order to make room for other circuit devices such as filters, the substrate height between the antenna and ground plane was designed to be 4 µm and fabricated by ourselves. The dimension of main parameters are $Sub\_h = 4\,\mu m$, $a = 2.2\,mm$, $b = 1\,mm$, $P\_l = 1.16\,mm$, $P\_w = 0.87\,mm$. The low-resistivity and high dielectric constant Si substrate is below the bottom metal layer M1. The patch size and the spacing between the patch and the edge were investigated to obtain the optimized miniature and high gain patch antenna. Other parameters such as the arguments of the feed-line are predetermined by demanded 50 Ω output impedance matching of the circuit and the chosen technology. The prototype of the designed patch antenna is shown in Figure 2.



(a) (b)

Figure 1: (a) The top-view and (b) cross-section of the designed on-chip antenna.

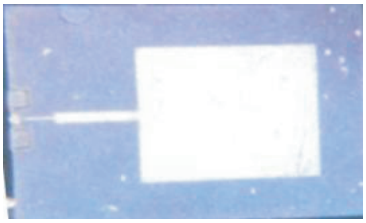


Figure 2: The prototype of the designed patch antenna.

3. RESULTS AND DISCUSSION

The simulated (blue line) and measured (red line) return loss results of the proposed antenna were shown in Figure 3. It can be seen that the resonance of the proposed antenna is around 62.85 GHz and the impedance bandwidth with $S_{11} < -10$ dB is from 62.25 GHz to 63.47 GHz. In comparison with the simulation results, the measured reflection coefficient offers a good match except for a 12.5% frequency shift. This may be due to the lower dielectric constant of the SiO_2 substrate and thinner epoxy glue layer on the antenna and the test board, thus leading to the lower resonant frequency.

The E-plane and H-plane radiation patterns of the designed antenna in the 4 μm SiO_2 substrate is displayed in Figure 4. The simulation results demonstrate the peak gain of the designed antenna is −10.3 dBi, which approached −2.69 dBi when the designed antenna is fabricated in the standard CMOS technology with 10 μm. The performance of proposed antennas as compared to other published on-chip antennas is presented in Table 1.

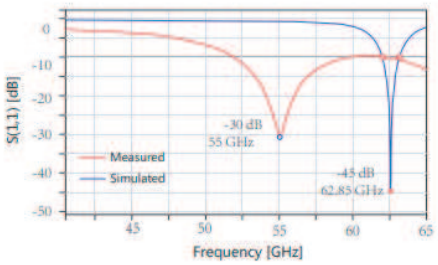
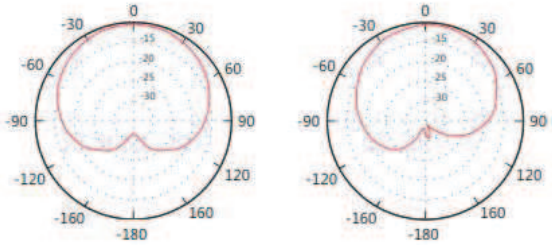


Figure 3: The simulated (blue line) and measured (red line) return loss results of the proposed antenna.



(a) (b)

Figure 4: (a) The E-plane and (b) H-plane radiation pattern of the designed antenna.

Table 1: The performance of the proposed antennas as compared to other published on-chip antennas.

Ref.	*Antenna Type*	*SiO_2 Substrate Height*	*Gain (dBi)*	*Area (mm^2)*
[3]	Dipole	9 μm	−8 dBi@21 GHz	3 mm × 0.5 mm
[4]	Inverted F	22 μm	−19 dBi@61 GHz	/
[5]	Yagi	/	−10 dBi@60 GHz	1.1 mm × 1.34 mm
[6]	Slot	12 μm	−2 dBi@140 GHz	1.2 mm × 0.6 mm
This work	Patch	4 μm	−10.3 dBi@60 GHz	0.87 mm × 1.16 mm
This work	Patch	10 μm	−2.69 dBi@60 GHz	0.87 mm × 1.16 mm

4. CONCLUSION

In this paper, a smaller occupation and higher gain antenna is designed by making detail analysis on the parameters of the on-chip microstrip antenna. The finally designed patch with 0.87 mm $*$ 1.16 mm occupies half of the area of the same patch antenna in traditional design method.

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