

Design of a Doherty Power Amplifier for Performance Enhancement

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Abstract— This work presents theory, design and simulation of an improved Power Amplifier (PA) based on the Doherty topology. It is theoretically shown that, using multiple iterations of source-pull and load-pull, a better main PA is accomplished. Taking into account that working conditions of the main and peak PAs affect the overall performance, the various performance indicators should be balanced. Optimal bias voltages are determined in the proposed DPA, providing higher efficiency both at full output power and at 6 dB back-off power, thus validating practical effects of the design and demonstrating a promising prospect to be used in the future wireless transmitter applications.

1. INTRODUCTION

Future wireless transmitters in the communication systems tend to be imposed more and more stringent constraints. To ensure that the communication transmitters could permit signal integrity upholding, base-station deployment operating cost reduction and an increase in battery life for mobile stations linearity and power efficiency are both crucial factors which must be considered in the design [1].

Improving the efficiency of the PA has been studied using efficiency enhancement techniques such as envelope elimination and restoration (EER), polar modulation, and envelope tracking (ET) [2–4]. These techniques could provide excellent efficiency performance using a complicated enveloped PA and/or switching PA, and high linearity performance can be achieved with the help of a digital predistortion technique.

Compared with technologies mentioned above, the Doherty Power Amplifier (DPA) stands out for its high efficiency, simple achievement, relatively low cost, small impact on the linearity system and other advantages. As well as its topology can be easily combined with the feed forward and predistortion techniques, the DPA has been widely studied and applied in the modern wireless communication systems.

2. DESIGN OF THE MAIN PA

The main PA is designed in this paper using an N-channel enhanced LDMOS tube MRF6S20010N of the Freescale Semiconductor with the center frequency of 2.14 GHz.

To guarantee a good performance the input and output matching sections are especially important in the design. So the optimum source impedance and load impedance should be found.

There is a platform which can provide templates of Load-Pull and Source-Pull simulations. By modifying the input signal power, scanning centers, scanning radius and sweep points, it is easy to get a team of equal efficiency circles and output power circles. Then we can obtain the optimum load impedance and source impedance according to the corresponding design requirements.

However, since source-pull and load-pull are divided into two separate steps to complete, it is probably that the source and load impedance end up not optimal. To solve this problem, the concept of multiple iterations is introduced into the design to achieve convergence solutions as follows [5].

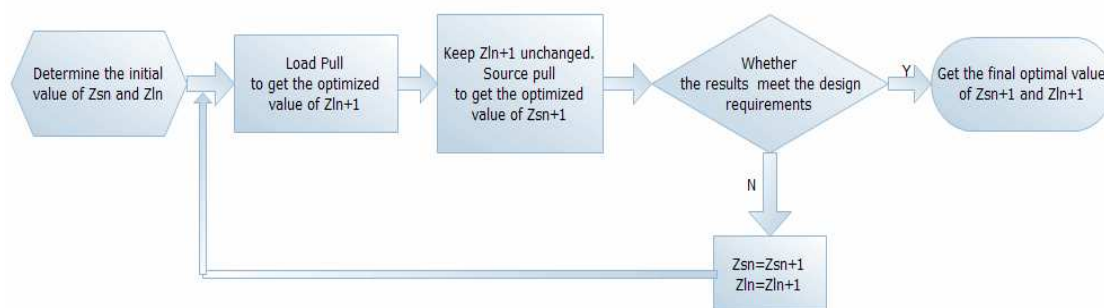


Figure 1: Flow chart of the multiple iterations using the source-pull and load-pull.

After several steps of multiple iterations, we get the optimum source impedance and load impedance. With the design of new matching circuits, an improved main PA is done. The new measured gain and power-added efficiency (PAE) are shown in Fig. 2, better than the results of single traction shown in the Fig. 3.

m1 indep(m1)=20.248 vs(P_gain_transducer,Spectrum[1])=18.248	m3 indep(m3)=37.863 vs(PAE,Spectrum[1])=36.146
m2 indep(m2)=41.703 vs(P_gain_transducer,Spectrum[1])=17.203	m4 indep(m4)=41.703 vs(PAE,Spectrum[1])=55.891

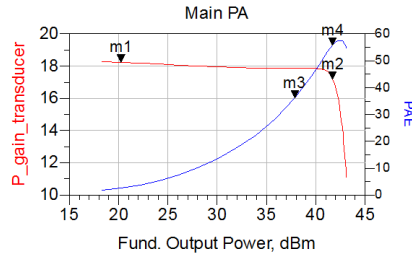


Figure 2: Simulation result after multiple iterations.

m1 indep(m1)=15.932 vs(P_gain_transducer,Spectrum[1])=15.932	m3 indep(m3)=38.001 plot_vs(PAE, Spectrum[1])=31.002
m2 indep(m2)=41.763 vs(P_gain_transducer,Spectrum[1])=14.763	m4 indep(m4)=41.763 plot_vs(PAE, Spectrum[1])=44.995

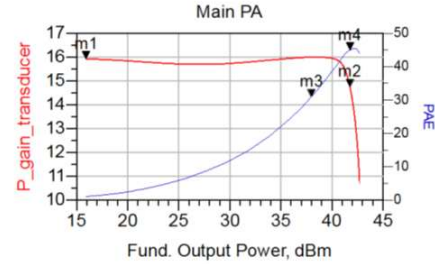


Figure 3: Simulation result before multiple iterations.

3. BASIC DESIGN OF THE WHOLE DPA

In this design, we use the inverted structure of Doherty mentioned in many literatures [6]. The compensation line after main PA is to enhance the drain resistance at small input power level to get earlier saturation and improve efficiency. The compensation line after peak PA is to transform small impedance into large impedance [7].

The transistors used for the main and peak PAs are identical in size and evenly driven. The main PA was biased in class AB condition and the peak PAs in class C. Using the Wilkinson power divider, we got the basic design.

4. FACTORS INFLUENCE ON THE PERFORMANCE OF THE DPA

In the DPA, efficiency and linearity are conflicting. In the area of low power levels, main PA works while peak PA is off, the overall linearity depends on the linearity of main PA. In the area of medium power levels, the participation of peak PA in Class C mode deteriorates the overall linearity. Only in the area of high power levels, the gain of main PA compresses while the gain of peak PA expands and then the effects just balances and makes improvement in the overall linearity. So based on the purposes of optimizing the DPA performance, the drain bias voltage of main PA and the gate bias voltage of peak PA are considered about that how to impact on the overall efficiency and linearity.

4.1. Drain Bias Voltage of Main PA

We know that main and peak PAs' drain bias voltages have a significant impact on the power back-off range and efficiency of the DPA. Based on the designed circuit above, sweeping and scanning the drain bias voltage of main PA from 25 V to 35 V by 2 V each step with other parameters unchanged, we can get the effect trends of gain and efficiency in Fig. 4, as well as the trends of linearity in Fig. 5.

As the simulation results shown above, since the drain bias voltage decreases, the main PA gets into saturation at a lower input power level, making efficiency at low power level greatly improved. But it is precisely because that the main PA unit gets into the saturated zone earlier, leading to the reduction of the gain and an overall deterioration of linearity at low power.

If we can properly reduce the drain bias voltage or dynamically adjust the drain bias voltage of the main PA unit according to the case of the input signal envelope, the efficiency of the PA will be greatly enhanced in a certain level of linearity.

4.2. Gate Bias Voltage of Peak PA

Gate bias voltage of the peak PA determines when it starts to work, so the gate bias voltage influences the linearity, gain, efficiency and other performance characteristics of the peak PA. The state of peak PA working in is mainly decided by the gate bias voltage. The lower gate bias voltage is, the "deeper" state of class C it works in.

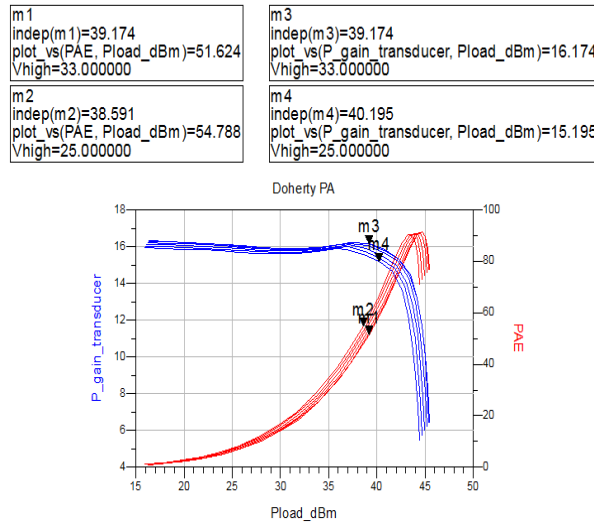


Figure 4: Trends of gain and efficiency.

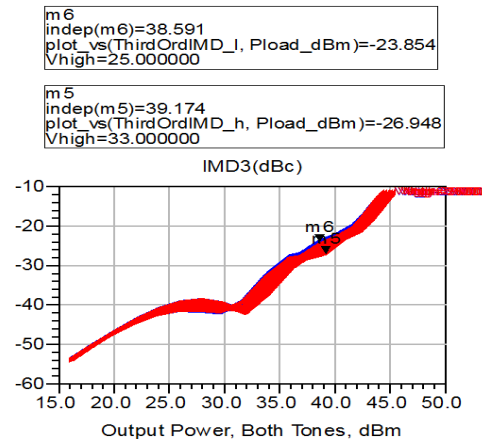


Figure 5: Trends of linearity.

The drain bias voltage of peak PA in this design ranges from 0.1 V to 2 V, stepping by 0.2 V. The scanning results of gate bias voltage of the peak PA are shown in Fig. 6 and Fig. 7.

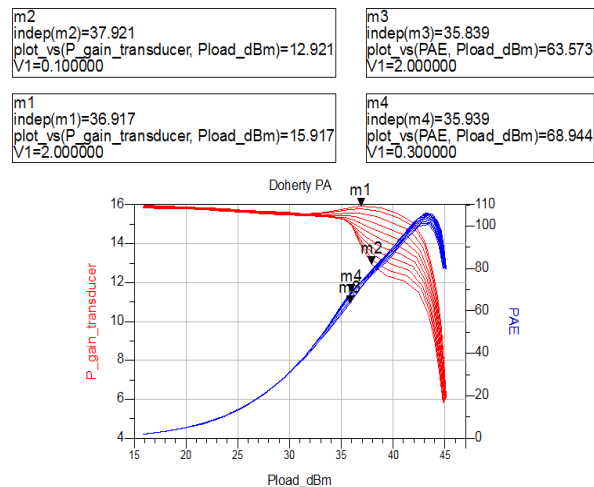


Figure 6: Trends of gain and efficiency.

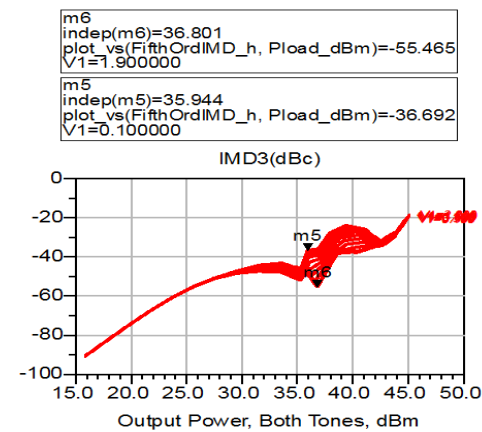


Figure 7: Trends of linearity.

According to the simulation results, the higher gate bias voltage is, the lower the starting point of peak PA. The inefficient operation state after its participation makes the total efficiency reduced. Therefore, the lower the gate bias voltage of peak PA is, the higher the efficiency can be while the worse the linearity will become.

5. IMPROVED DESIGN OF THE WHOLE DPA

Considering the impact of factors mentioned above on the overall performance of the DPA a balanced choice according to the actual needs of the various performance parameters is proposed. We make the main PA working in AB condition with a drain bias voltage of 28 V and the peak PA in a proper C condition with a gate bias voltage of 1.96 V. With other optimizations not described in detail, the final improved DPA is completed. The results are shown in the Fig. 8. Compared with the results shown in the Fig. 9 before improvement, the PAE at saturation point and 6 dB back point have greatly improved, while the gain and linearity still meet the design requirements without deterioration.

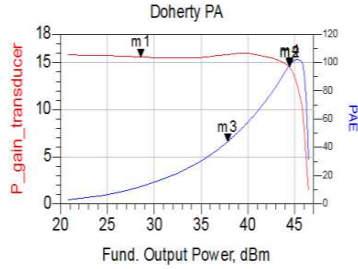
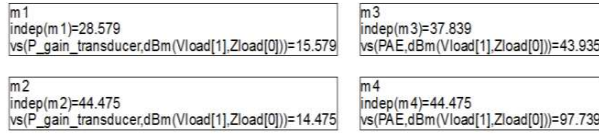


Figure 8: Results after improvement.

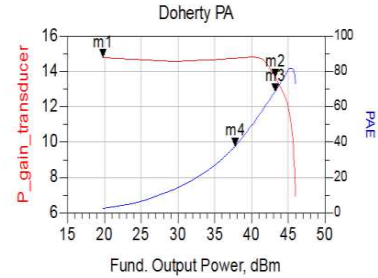
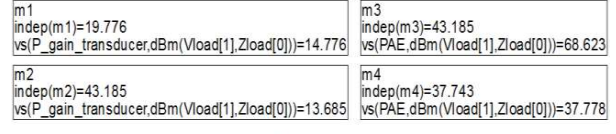


Figure 9: Results before improvement.

6. CONCLUSION

In this paper, an improved design of Doherty PA has been proposed. The design is based on the use of multiple iterations of source-pull and load-pull and a balanced consideration of the state of bias. The simulation results show that the proposed Doherty PA has a power-added efficiency (PAE) much higher than the traditional one with other performances not deteriorated.

REFERENCES

1. Gustafsson, D., C. M. Andersson, and C. Fager, "A novel wideband and reconfigurable high average efficiency power amplifier," *Microwave Symposium Digest (MTT)*, Vol. 17, 169–178, Department of Microtechnology and Nanoscience, Chalmers University of Technology, Kemivägen, 9, Göteborg SE-412 96, Sweden, 2007.
2. Raab, F. H., B. E. Sigmon, R. G. Myers, and R. M. Jackson, "L-band transmitter using Kahn EER technique," *IEEE Trans. Microw. Theory Tech.*, Vol. 46, No. 12, 2220–2225, Dec. 1998.
3. Chen, J.-H., P. Fedorenko, and J. S. Kenney, "A low voltage W-CDMA polar transmitter with digital envelope path gain compensation," *IEEE Microw. Wireless Compon. Lett.*, Vol. 16, No. 7, 428–430, Jul. 2006.
4. Kimball, D. F., J. Jeong, C. Hsia, P. Draxler, S. Lanfranco, W. Nagy, K. Linthicum, L. E. Larson, and P. M. Asbeck, "High-efficiency envelope tracking W-CDMA base-station amplifier using GaN HFETs," *IEEE Trans. Microw. Theory Tech.*, Vol. 54, No. 11, 3848–3856, Nov. 2006.
5. Liu, Y. and H. B. Xiao, "Design and simulation of an improved Doherty power amplifier," *IEEE Trans. Applied Mechanics and Materials*, Vol. 496–500, 1109–1112, 2014.
6. Yang, Y., J. Cha, B. Shin, and B. Kim, "A fully matched N-way Doherty amplifier with optimized linearity," *IEEE Trans. Microw. Theory Tech.*, Vol. 51, No. 3, 986–993, Mar. 2003.
7. Zhao, H. M., "Design on high-power amplifier module of communication," 2013.