Evaluation of Power Transistors Figure of Merit for Hard Switching Commutation Mode through Experimental Analysis

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Abstract— Nowadays demand for efficiency and high density of electronic device is high. Therefore, great emphasis is placed on the properties of electronic components such as diodes, transistors, transformers and more. Hence the scientific discipline was created Figure of Merit (FOM) which is dealing with this issue.

The proposed article deals about the analysis of FOM of several power MOSFETs, whereby main parameters are taken into consideration for calculation purposes. In order to verify faithfulness of FOM the experimental measurements for determination of switching as well as conduction losses of selected transistors are performed. Because experimental analysis represents time-consuming process for evaluation of transistor switching performance, the various FOM methodologies are being described taking into account main parameters for the FOM evaluation (transistor parasites, gate charge, switching frequency, parameters of target application, e.g., voltage — current ratings). Comparisons between the amount of transistor's losses and its FOM indicator are provided.

1. INTRODUCTION

The development of switched mode power supplies significantly moved forward. Requested parameters of switched mode power supplies (SMPS) are reduction of the size and reduction of power losses (increase of efficiency). In this article we decided to analyze several methods of FOM for the power MOSFET transistors. These methods are:

- Switching FOM.
- Conduction FOM.
- Detailed FOM.
- Johnson FOM.

FOM is numeric value representing power parameter of components and other important factors, which affect this parameter. If we want to work with FOM method it's very important to know internal parasitic parameters. MOSFET transistors, through unipolar structure, belong to the fastest power semiconductor component. Dynamic parameters are limited by internal parasitic components [1–4]. The values of these parameters are given in components datasheets and are dependent on the internal structure of MOSFET and on its technology (manufacture). Selected transistors for FOM evaluation as well as experimental analysis of hard-switching commutation mode are CoolMOS IPW60R165CP, CoolMOS, SPP20N60C3 and MOSFET IRF840. The last mentioned device represents older technology of MOSFET transistors, whereby CoolMOS transistors exhibits currently best in class performance for power applications (for example solar inverters, renewable energy, telecom/servers, front-end converters etc.…).

2. FOM FOR MOSFET TRANSISTORS

2.1. Switching FOM

Switching FOM is used to evaluate switching behaviour/performance. Next formula is valid for calculation:

$$\mathrm{FoM}_{SW} = R_{DS(ON)} * Q_{GD}, \tag{1}$$

where

- Q_{GD} is main parameter of turn-on loss.
- $R_{DS(ON)}$ represents conduction losses, when transistor is in on-state.

Some manufactures indicates the value of Q_{SW} or Q_{GS2}. In this case we can find more accurate value of FOM_{SW} (2).

$$\mathrm{FoM}_{SW} = R_{DS(ON)} * (Q_{GD} + Q_{GS}), \tag{2}$$

where

- Q_{SW} is representing sum of turn-on loss (related with $Q_{GD} + Q_{GS}$.
- Q_{GS} is gate charge between threshold voltage and Miller plateau.

2.2. Conduction FOM_{CON}

This is a traditional MOSFET FOM and determines rectified power loss. FOM_{CON} (3) represents the conduction losses and power losses of the transistor's gate electrode.

$$\mathrm{FOM}_{CON} = \left(R_{DS(ON)} * Q_G\right) \tag{3}$$

For soft switching technique Q_{GD} is negligible and therefore we would like to reduce $R_{DS(ON)}$ in order to improve efficiency. On the other side, with reduction of $R_{DS(ON)}$, Q_G loss increases. There exist also better method which utilizes parameters Q_{OSS} (Output charge) and Q_{RR} (Reverse recovery charge) together with Q_G for evaluation of power loss. In most cases, switching performance is mostly missing; therefore combination with Q_{SS} is sometimes omitted in which conditions have no standards too. The eGaN transistors are Q_{RR} and Q_{OSS} negligibly small as compared to silicon MOSFETs [5].

2.3. Detailed FoM

If it is necessary to evaluate the performance of the transistor in terms of more precise choice, then more detailed information are needed where effect of turn-on, turn-off, conduction loss and loss due to gate excitation of transistor are considered (4).

$$\begin{aligned} P_{loss} = {} & \frac{U_{in} \cdot I_o}{2} \cdot \frac{(Q_{GD} + Q_{GS}) \cdot R_G}{(U_{GS} - U_{PLT})} \cdot f_{SW} + \frac{U_{in} \cdot I_o}{2} \cdot \frac{(Q_{GD} + Q_{GS}) \cdot R_G}{U_{PLT}} \cdot f_{SW} \\ & + I_o^2 R_{DS(ON)} \frac{U_o}{U_{IN}} + Q_G U_{GS} f_{SW}, \end{aligned} \tag{4}$$

where

- U_{PLT} is leading voltage of gate drive,
- I_O is nominal value of current taken from datasheet,
- f_{SW} is nominal switching frequency.

Furthermore, it is necessary to adopt new value namely excitation losses in gate circuit K_{GS} (5).

$$K_{GS}(U_{DR}) = 1 + \frac{U_{DR}}{U_{PLT} - U_{TH}} \cdot \frac{2U_{PLT}(U_{DR} - U_{PLT})}{U_{IN} I_o R_G}, \tag{5}$$

where U_{DR} is value of excitation voltage and U_{TH} is threshold voltage. After that it is possible to calculate FOM parameter for hard switching commutation mode (6). In the following equation consideration of the losses of individual components is accepted [6–9].

$$\mathrm{FOM} = (Q_{GD} \cdot + K_{GS} Q_{GS}) \cdot R_{DS(ON)} \tag{6}$$

2.4. Johnson FoM

This method is for broadband gap devices like GaN transistors. Present type of transistor has desired properties for high power application such as size of band gap and thermal conductivity. Johnson value represents high frequency power of wide-energy devices and is proportional to saturation time and to the critical value of the electric field as shown in the following Formula (7).

$$\mathrm{FOM}_{\mathrm{johnson}} = \frac{v_{sat} E_{BD}}{2\pi}, \tag{7}$$

where

- v_{sat} represents speed of saturation.
- E_{BD} is the electric field which initiates the ionization.

However the value of FOM is not to be easily experimentally verified, because both parameters v_{sat} and E_{BD} are intrinsic properties of the components. On the other side it is possible to find these parameters by the simulation. These values can be coupled to the microwave measurements. In general the cut-off frequency f_t is associated with an effective speed of saturation, which can be calculated by Equation (8).

$$f_T = \frac{v_{sat}}{2\pi L_G}, \tag{8}$$

where

- L_G is effective length of gate.

Based on experimental analysis, it can be determined that the gate field varies almost linearly across the effective length of the gate. Visible change mainly occurs mostly at the end of turn-off interval. Since potential losses occur in the space between gate electrode and contacts we can write the equation for the breakdown voltage [6–9].

$$V_{BD} = \alpha \frac{E_{BD} L_G}{2}, \tag{9}$$

where

- α is an adjustable parameter which is associated with the voltage drop across the gate to the rated voltage of the device.

Therefore, we can rewrite the FOM within the experimentally determined parameters with the use of following Equation (10).

$$\mathrm{FOM}_{\mathrm{Johnson}} = \frac{1}{2\pi} \left(2\pi L_G f_T\right) \frac{2V_{BD}}{\alpha L_G} = \frac{2}{\alpha} f_T V_{BD} \tag{10}$$

The parameter α can be extracted directly from the measurement or simulation using the Formula (10) and the calculation of the breakdown voltage as integral field over the channel on which the first impact ionization occurs.

3. EVALUATION OF FOM OF SELECTED TRANSISTORS

Determination of FOM parameter of selected transistors was done with the use of methodology A — switching FoM (2), where effect of Miller capacitance is also considered. Conduction FoM has been evaluated with the use of (3), where Q_{RR} was also accepted. The results of calculations are shown in Table 1. As can be seen, the lowest value of switching and conduction FOM parameter is for IPW60R165CP transistor (the lower the value is the better performance of transistor may be achieved).

Table 1: Figure of merit for methodology A and B.

	FOM$_{SW}$	**FOM$_{CON}$**
IPW60R165CP	3,31	6,97
SPP20N60C3	8,36	18,62
IRF840	24,65	39,61

Table 2: The circuit and transistor parameters for FoM evaluation based on methodology C.

	U_{TH} [V]	U_{DR} [V]	U_{PLT} [V]	I_O [A]	U_{IN} [V]	R_G [Ω]
IPW60R165CP	3	15	5	variable	400	1.9
SPP20N60C3	3	15	5.5	variable	400	0.54
IRF840	4	15	5	variable	400	9.1

Table 3: Parametrical evaluation of figure of merit for hard switching based on methodology C.

U_{in} = 400 V	IPW60R165CP		SPA20N60C3		IRF840	
I [A]	K_{GS}	FOM	K_{GS}	FOM	K_{GS}	FOM
1	1.99	4.63	3.90	14.43	1.41	27.10
2	1.49	3.97	2.45	11.39	1.21	25.88
3	1.33	3.74	1.97	10.38	1.14	25.47
4	1.25	3.63	1.73	9.88	1.10	25.26
5	1.20	3.57	1.58	9.57	1.08	25.14
6	1.16	3.52	1.48	9.37	1.07	25.06
7	1.14	3.49	1.41	9.23	1.06	25.00
8	1.12	3.47	1.36	9.12	1.05	24.96
9	1.11	3.45	1.32	9.03	1.05	24.92
10	1.10	3.43	1.29	8.97	1.04	24.90

On the other side, if we need to evaluate selection of transistor more complexly, then it is necessary to consider also gate drive loss K_{GS} (5). This part becomes very important when very-high frequency operation is considered. Input values for calculation of detailed FoM as well as for calculation of K_{GS} listed in Table 2. Consequently the evaluation of FOM was made parametrically, i.e., in dependency on the parameters that are influencing hard-switching commutation mode in the most manners (switching frequency, load current). It must be said, that all FOMs have been computed for main circuit variables, at which experimental measurements were provided (Table 3).

As can be seen, the value of FoM from Table 2 is higher compared to FoM_{SW}, because losses from gate drive are taken into account too.

As can be seen from previous results IPW60R165CP is showing best performance, when complex and simple FOM has been calculated. When we look more in detail on the results from Table 3 it can be seen that IPW60R165CP is showing relatively small difference in the value of FOM, when change of transistor current is being considered. This can be explained in the way that internal capacitive parasitic components together with circuit and transistor parameters results in suitable value. IRF840 shows the best value of K_{GS}. However, internal parasitic components are decreasing qualitative indicator of this part markedly, thus utilization for high-end systems won't be a good choice.

Let's see if these results would also be confirmed after experimental analysis of hard-switching commutation mode.

4. EXPERIMENTAL ANALYSIS OF HARD-SWITCHING COMMUTATION MODE

The experimental analysis served for the analysis of dynamic properties during hard-switching of selected power transistors, whose selected type for analysis are CoolMOS IPW60R165CP, CoolMOS, SPP20N60C3 and MOSFET IRF840. The experimental analysis for FOM evaluation has been realized at these parameters:

- $U_{DC} = 400\,\mathrm{V}$.

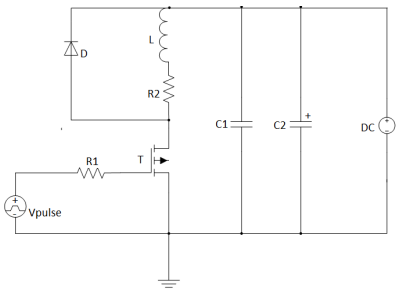

Figure 1: Pricnipal schematic for experimental analysis of hard-switching.

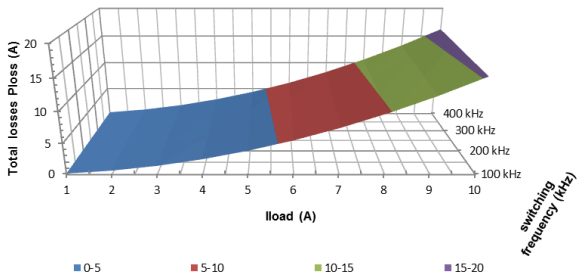

Figure 2: Pricnipal schematic for experimental analysis of hard-switching.

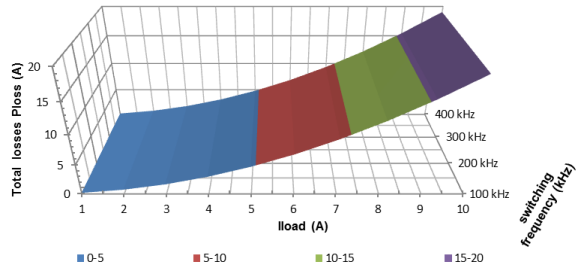

Figure 3: Pricnipal schematic for experimental analysis of hard-switching.

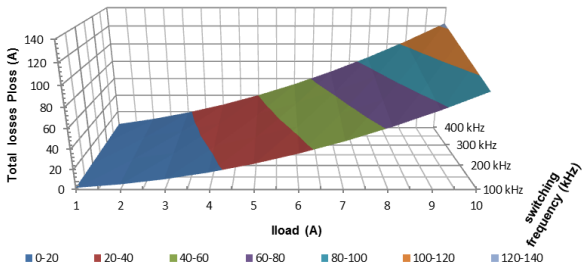

Figure 4: Pricnipal schematic for experimental analysis of hard-switching.

- $I_{load} = 1$–$10\,\mathrm{A}$.
- $f_{sw} = 100$–$400\,\mathrm{kHz}$.

Principal schematic for the analysis is shown on Figure 1. The experimental analysis as well as FOM evaluation was made parametrically, i.e., in dependency on the parameters that are influencing hard-switching commutation mode in the most manners (switching frequency, load current).

Figure 2 to Figure 4 are showing results from parametrical experimental analysis of switching performance of transistor (evaluation of transistor's switching power losses) in dependency on transistor's current and switching frequency. Each transistor was investigated separately with the use of universal testing device and automatic switching loss evaluation algorithm, whereby each part of power loss has been evaluated independently, i.e., turn-on loss, conduction loss and turn-of loss [11–17].

Experimental measurements show that IPW60R165CP is achieving best switching performance in the whole investigated range of variables. Based on these results, it can be said that evaluation of FOM gives credible information about the quality of transistor performance for target application. Also, in order to improve qualitative indicators of modern SMPS, detailed FOM evaluation, where circuit parameters are being considered, gives proper information that can be sufficient during selection of proper power transistor structure.

Because the research and development process must be continuously accelerated (due to market requirements), the FOM methodology seems to be very valuable and perspective procedure for transistors quality evaluation.

5. CONCLUSION

The main aim of this paper was confirmation of FOM methodologies for the evaluation of the quality of power transistors from "efficiency" point of view. For this purpose the parametrical evaluation of detailed FOM was provided for several generations of MOSFET transistors. The confirmation of FOM results was provided in the way of experimental analysis of switching power losses during hard switching commutation mode. The measurements for each transistor were evaluated separately and switching losses in dependency on transistor's current and on switching frequency were calculated. The value of FOM is a power merit of devices, whose value indicates quality of semiconductor device. The lower this value is, the better the performace shall be. After comparisons between results of experimental analysis and results from FOM calculation, it can be said, that FOM methodologies presents very perspective solution for the selection of proper power device for selected power application.

In future works, we would like to focus on the evaluation of FOM parameter for soft-switching commutation modes (zero-voltage switching, zero-current switching) as well as on determination of FOM for various power devices (diodes — SiC, GaN transistors etc.…). Consequently the quality indicator of proper semiconductor structures, will be verified during operation of target application system (e.g., SMPS for distributed systems), where system efficiency will be the most important merit.

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REFERENCES

1. Deboy, G., N. Marz, J. P. Stengl, H. A. S. H. Strack, J. A. T. J. Tihanyi, and H. A. W. H. Weber, "A new generation of high voltage MOSFETs breaks the limit line of silicon," *International Electron Devices Meeting, IEDM '98, Technical Digest*, 683–685, 1998.
2. Hudgins, J. L., G. S. Simin, et al., "An assessment of wide bandgap semiconductors for power devices," *IEEE Transactions on Power Electronics*, Vol. 18, No. 3, May 2003.
3. Lu, B., W. Dong, Q. Zhao, and F. C. Lee, "Performance evaluation of CoolMOS/sup/spltrade// and SiC diode for single-phase power factor correction applications," *Eighteenth Annual IEEE Applied Power Electronics Conference and Exposition, APEC' 03*, Vol. 2, 651–657, 2003.
4. Baliga, B. J., "Power semiconductor device figure of merit for high frequency applications," *IEEE Electron Device Lett.*, Vol. 10, 455–457, 1989.
5. Johnson, A., "Physical limitations on frequency and power parameters of transistors," *RCA Review*, Vol. 26, 163–177, 1965.
6. Kim, I., S. Matsumoto, T. Sakai, and T. Yachi, "New power device figure of merit for high-frequency applications," *Proc. Power Semiconductor Devices and ICs*, 309–314, 1995.
7. Brown, J. and G. Moxey, "Power MOSFET basics: Understranding MOSFET characteristiks associated with the figure of merit," *Vishay Siliconix*, Sep. 8, 2003.
8. Strydom, J., "eGaN(tm) — Silicon power shoot-out: Part 1, Comparing figure of merit (FOM)," EPC, Sep. 1, 2010.
9. Frivaldsky, M., "Topologicka optimalizácia LLC Meniča," Univerzita of Zilina, 2013.
10. Frivaldský, M., P. Drgoňa, and P. Špánik, "Experimental analysis and optimization of key parameters of ZVS mode and its application in the proposed LLC converter designed for distributed power system application," *Electrical Power and Energy Systems*, Vol. 47, 448–456, 2013, ISSN: 0142-0615.
11. Frivaldský, M., P. Drgoňa, and P. Špánik, "Hard switching process optimization for selected transistor suited for high power and high frequency operation," *Journal of Energy and Power Engineering*, Vol. 4, No. 12, 2010, ISSN: 1934-8975.
12. Špánik, P., M. Frivaldský, P. Drgoňa, and J. Kandráč, "Efficiency increase of switched mode power supply trough optimization of transistor's commutation mode," *Elektronika IR Elektrotechnika*, Vol. 105, No. 9, 49–52, 2010, ISSN: 1392-1215.
13. Kindl, V., T. Kavalir, R. Pechanek, B. Skala, and J. Sobra, "Key construction aspects of resonant wireless low power transfer system," *ELEKTRO 2014*, 303–306, May 19–20, 2014.
14. Brandstetter, P., P. Chlebis, and P. Palacky, "Application of RBF network in rotor time constant adaptation," *Elektronika IR Elektrotechnika*, Vol. 113, No. 7, 21–26, 2011.
15. Grman, L., M. Hrasko, and J. Kuchta, "Single phase PWM rectifier in traction application," *Journal of Electrical Engineering-Elektrotechnicky Casopis*, Vol. 62, No. 4, 206–212, Aug. 2011.
16. Ferkova, Z., M. Franka, and J. Kuchta, "Electromagnetic design of ironless permanent magnet synchronous linear motor," *International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*, 721–726, Italy, Jun. 11–13, 2008.
17. Kovacova, I. and D. Kovac, "Inductive coupling of power converter's EMC," *Acta Polytechnica Hungarica*, Vol. 6, No. 2, 41–53, 2009.