Realization of a Compact High Speed Mass Storage System

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Abstract— Conventional on-board storage systems are often weighty, large and high power consumption, which can't meet the requirement of the miniature airborne synthetic aperture radar (SAR) system. A new data storage system, integrated with SAR signal processor, is presented in this paper. The compact flash (CF) card and the FPGA are used as storage medium and the host respectively, in the data storage system. However, the major problem of high speed data storage is the irregular write response time due to the internal overhead in the card and frequently cluster switching involving retrieving and updating of cluster connection information. Two methods are presented in this paper to solve the problem. The first one is that the DDR3 flashes connecting with the DSP are iteratively used as the buffer of the SAR data. Another method is that all the available clusters are pre-allocated at once when the files are created. To verify our proposal, the prototype data storage system is implemented on a signal processing board and a CF card with the capacity of 128 GB. The added size, weight, and power consumption for the data storage are really small. Moreover, the data writing rate is over 100 MB/s. As a consequence, the system achieves our goal successfully in that storage system of the miniature SAR is compact, high speed and large capacity.

1. INTRODUCTION

There is a growing interest in lightweight cost-effective synthetic aperture radar (SAR) with the fast image generation capacity and even small enough to be mounted on a miniature aerial vehicles (AVs). This demands for the compact SAR components. With ongoing bandwidth growing of the beat spectrum of the SAR, the compact storage system with the capacity of the high speed mass storage is acute needed in some applications where the bandwidth of the data links is limited.

At present, the hard magnetic disk, solid-state disk, flash and CompactFlash (CF) card are the usual mediums for the data storage [1]. The CF card is the most suitable medium for the data storage of the SAR data due to its high data transfer rate, small dimension, large capacity, easily be upgraded, shock resistance and other features [2]. Based on the CF card, this paper addresses the design of the high speed mass storage. It should be mentioned that the prototype of the storage system is a real-time SAR imaging processor which includes ADC, FPGA, DSP, and CF card, as shown in Figure 5. The SanDisk Extreme Pro CF card with the capacity of 128 GB is the high speed storage medium; the Xilinx Virtex-6 XC6VLX75T type FPGA is used as the host of the CF card; the TI TMS320C6678 DSP is used for signal processing. The data storage system can achieve the data transfer rate of 100 MB/s.

2. SYSTEM DESIGN

As the capacity of the CF card increases up to 128 GB, the FAT file system, which has simple architecture and a higher compatibility with other systems, is needed to manage the storage effectively [4, 5]. The FAT file system contains four major parts: Master Boot Record (MBR), Dos Boot Record (DBR), File Allocation Table (FAT) and DATA region. These four parts contain the boot codes, system parameters, data cluster interconnection information, and data of the files, respectively.

There are two obstacles for the demand of the high speed of the data storage. The first one is the internal overhead, such as the operation of erasing the content of the sectors is needed before the sectors write operation of the CF card. The time of such implicit operation is relatively long and can't be predicted precisely. Another obstacle is the frequently cluster switching that the data writing of a new cluster needs a series of operations, such as retrieving and updating of cluster connection information in FAT, which produce irregular response times, especially for the data writing with large size. Follows are implementation architecture of the data storage and relatively methods to overcome these two obstacles.

2.1. Data Flow

The article addresses the data flow of the data storage/signal processing integrated system, as shown in Figure 1. The FPGA fetches the raw data from the A/D converter and preprocesses these data to generate the base band data (preprocessed data), the sample rate of which is much lower than that of the raw data. Then the preprocessed data is feed to the DSP. For the image data storage, the DSP generates the resulting image data and sends the imaging data to the DDR3 flashes connecting with DSP. For the preprocessed data storage, the DSP doesn't process the received data and just sends these data to the DDR3 flashes. Finally, the SAR data is read from the DDR3 flashes by the DSP and sent back to the FPGA when the SAR data could be wrote into the CF card by the FPGA.

To meet the demand of high data transfer rate, the SRIO interface between the FPGA and the DSP, and the DDR3 interface between the DSP and the DDR3 flashes, are used for data transfer. The bandwidth of the SRIO is 5 Gbps and the DDR3 can reach the data transfer rate over 10 GB/S, which are all much faster than the maximum data writing rate (150 MB/s now) of the CF card. In order to solve the problem of the mismatch of the data rate between the SRIO and the CF card, two FIFOs in the FPGA are added as the buffers of the SAR data.

2.2. Implementation Architecture

Based on the flow chart of data storage/signal processing integrated system in Figure 1, the data storage contains two types of process. The first process consists of data transfer that SAR data is transferred from the DDR3 flashes to the FPGA, and the data reading/writing of the CF card. Another process is control logic, whose primary function is controlling the flow of the first process. As a consequence, the implementation of the data storage could be divided into two channels. The first one is the data channel that is made up of the data transfer unit and the CF card read/write unit which has six subunits: the DBR and MBR read unit, FAT read unit, FAT write unit, FDT read unit, FDT write unit, and data write unit. Figure 2 illustrates the implementation architecture of the data storage. To get the SAR data, the data transfer unit transfers the SAR data (preprocessed or imaging data) from the DDR3 flashes to the FPGA. Finally, the six subunits of the CF card read/write unit implement parameters searching, the cluster connection retrieving and updating, the file directory retrieving and updating, and the data writing to the CF card, respectively. The schematic of the FPGA implementation for the data transfer unit and the CF card read/write unit are shown in Figure 3 and Figure 4, respectively.

In the control channel, there are five sub-controllers: the data transfer controller, DBR and MBR read controller, FAT read/write controller, FDT read/write controller and data write controller. The first sub-controller controls the operations of the data transfer. The other sub-controllers form the file system controller, which controls the CF card read/write operation to store data in the form of FAT32 file system.

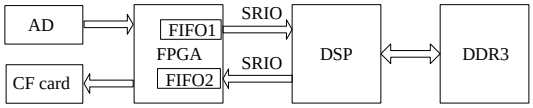


Figure 1: The data flow of the storage system.

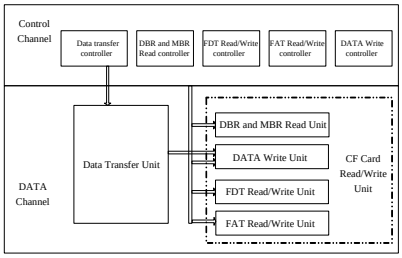


Figure 2: The FPGA implementation architecture of the data storage.

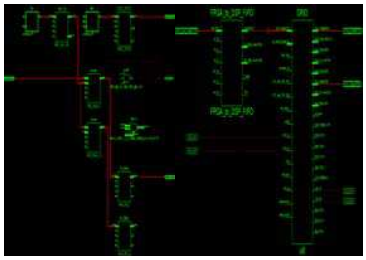


Figure 3: The schematic of the implementation about data transfer unit.

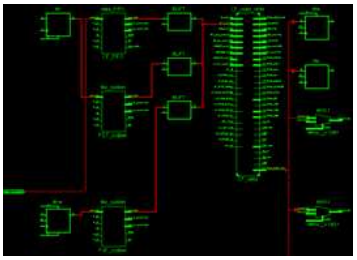


Figure 4: The schematic of FPGA implementation about CF card read/write unit.

2.3. High Speed Design

For the first obstacle for the high speed data storage, the long and unpredictable write preparing time is a vital problem. The preparation time is not fixed, usually within 700 µs, but occasionally abnormal time can reach 60 µs. Assume the data transfer rate is 80 MB/s, the data buffer with capacity of at least 4.8 MB is required. However, the capacity of 4.8 MB is much larger than that of the memory in the XC6VLX75T FPGA, with the RAMs of 700 KB. The way to expand the memory of the FPGA, at first glance, is that the large capacity buffer, such as the Static RAM [6], FIFO and Dynamic RAM, connects with the FPGA. But the complexity, size and power consumption of data storage system will be increased. As the matter of fact, the buffer already exists: the DDR3 Flashes with very large capacity has been connected with the DSP, as shown in Figure 1. If this large capacity memory can be used as the FPGA's buffer, whatever the design and the implementation of the storage would be very compact. Fortunately, the answer is positive. As we noticed in Figure 1, the FPGA is connected with the DSP via SRIO. The buffer to the DSP is completely transparent for the FPGA through the SRIO interface. In other words, the FPGA can access the buffer of the DSP.

For the second obstacle of the high speed data storage that the FAT32 file system requires frequently retrieving and updating of the cluster connection and the file directory, the procedure is so complex that it may influence the stability of system and take relatively long time as well. In this paper, the method called file system pre-allocation is adopted to reduce the switching overhead in the FAT file system operation. Firstly, all data is stored orderly in the DATA region of CF card, which makes the cluster connections ordinal in the FAT as well. Secondly, the size and name of files are constrained in a certain rule, which can make it possible that omitting the operation of information retrieving in the FAT and FDT, because the cluster connection information of all files is clear according to rule. Thirdly, all available clusters are pre-allocated in the FAT according to the rules we made once the storage procedure starts. So the file can be written without further operation of cluster allocation.

3. EXPERIMENT

To evaluate the performance of data storage system, we have implemented the data storage system in the prototype of the SAR real-time processor, as shown in Figure 5. Yellow marked parts are the key devices of the data storage system: CF card, FPGA, DDR3 Flashes and DSP. The added size for the data storage is quite small, about 60 mm × 41 mm × 2 mm and the added weight is no more than 70 grams.

The capacity, speed and power consumption are the key parameters of storage system. Obviously, the capacity of storage system equals that of CF card, about 128 GB. Based on the flow chart of the data storage/signal processing integrated system, the data transfer rate of the SRIO interface and the DDR3 interface, and data writing rate of the CF card are three restriction factors for the speed of the CF card. As a consequence, their data rates needed to be tested on the data storage system.

The data rates of the SRIO and DDR3 interface are all independent of the data transfer direction. In the test of the data transfer rate of the SRIO interface, the data with different count is generated by the FPGA and transferred to the DSP through the SRIO interface. The DSP measures the time and validates the correctness of the data. The result of the DSP indicates all transferred data is

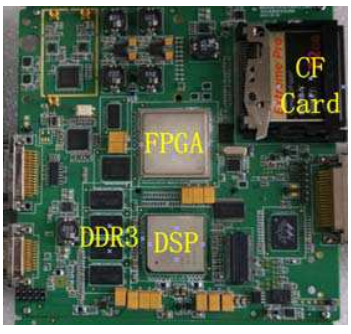
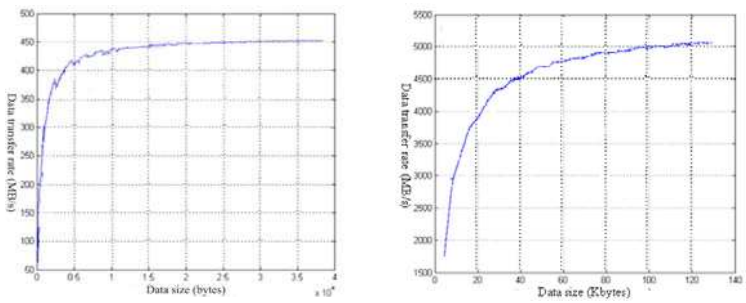


Figure 5: Hardware platform of data storage system.



(a) (b)

Figure 6: Data transfer rate of SRIO and DDR3 interface. (a) Data transfer rate of SRIO. (b) Data transfer rate of DDR3.

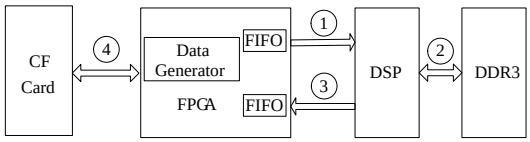


Figure 7: Flow chart of experiment.

correct. The data transfer data rate reaches about 452 MB/s when the data count is 32 KB and keeps steadily as the count of data increases, as shown in Figure 6(a).

For test of the data transfer rate of the DDR3 interface, the DSP generates the data with different count and sends the data to the DDR3 flashes, and measures the transfer time. Then the data stored in the DDR3 is read by the computer through the DSP emulator and validated by the computer. The result indicates the data is all correct. Figure 6(b) shows the data transfer rate of the DDR3, which reaches about 5032 MB/s when the data count is 120 KB and keeps steadily as the count of data increases.

Figure 7 illustrates the flow chart of the speed test of the data storage system. The data with the capacity of 8 GB generated by the FPGA in the sustained rate of 100 MB/s and sent to the DSP though the SRIO interface. The DSP fetches the data and sends them into the DDR3 Flashes. Then the data in the DDR3 is read by the DSP and transferred to the FIFO of the FPGA when the CF card starts to store the data. Finally the data is written to the CF card. The data in the CF card is read and validated by the Computer. The result indicates that the data stored in the CF card is same as that of the data generator in the FPGA. So the maximum transfer rate of storage system is more than 100 MB/s.

The total power consumption of the data storage/signal processing system is about 18 W and the power for implementing the function of signal processing is more than 16.8 W in the temperature of $18^0\circ$C. As a consequence, the add power consumption for the data storage is no more than 1.2 W.

4. CONCLUSION

The design of data storage system with high speed and large capacity is presented and implemented in the prototype of SAR real-time processor in this paper. The CF card is used as the basic medium and the FPGA is as its host in the storage system. The DDR3 flashes connecting with the DSP are used to make up the disadvantage of the CF card, of which the write response time is irregular. The method of file system pre-allocation is presented to solve the switching overhead problem of FAT32 file system. According to the experimental test of storage system, the system achieves our goal successfully in that storage system of the miniature SAR is compact, high speed and large capacity.

It is pointed that the storage system can also be easily modified to be a SAR data re-player where the preprocessed SAR data stored in the CF card is read by the FPGA and then transferred to the DSP to generate the imaging data. This function is very useful for the test of the SAR imaging algorithm. Moreover, CF card with higher data writing rate and larger capacity can be used in this system without modifying any hardware. In other words, this storage system could be upgraded in future.

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