Generic InP-based Integration Technology: RF Crosstalk in High-capacity Optical Transmitter PICs

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(*Invited Paper*)

Abstract— This paper reviews the basic ideas behind generic photonic integration and outlines how high-capacity integrated optical transmitters can benefit from this approach. Measurements of electrical coupling effects in a packaged transmitter chip are given, showing 2 dB power penalty due to RF crosstalk. A suitable simulation method for analyzing coupling effects on the integrated chip is presented and used to investigate the crosstalk originating from on-chip electrical routing lines and electro-optical phase shifters.

1. INTRODUCTION

Photonics is regarded by many as an enabling technology of the 21st century and it is been applied in many application areas such as in telecommunications, sensing and in the healthcare field. Similar to electronic integrated circuits, optical components and functionalities can also be combined together on one single, small form-factor chip, leading to a photonic integrated circuit (PIC). In the photonics industry, PIC based solutions are gaining popularity due to their small size, low cost and added functionality and value. However, development of the necessary integration technology is costly and time-consuming, as it is usually specifically tailored to the desired application and not easily transferable to others. This also restricts the access to photonic integration technology to a small group of preferential users. The recent emergence of generic photonic integration based on a foundry model approach aims at solving this issue by providing a few integration technologies that can realize a broad range of functionalities and by offering its access to a wide user range at low cost [1]. One of the traditional drivers of PIC development lies in the field of optical communications, where high-capacity wavelength-division multiplex (WDM) transmitters and receivers are needed to keep up with the increasing bandwidth demand. High-performance and large-scale photonic integrated circuits (LSPIC) coming from optimized integration processes has been the state-of-the-art solutions up until now [2], but could be replaced by lower-cost PICs in future created using generic integration technology. To maintain a high performance and its competitiveness and at the same time keep costs low, generic integration technology has to address certain challenges in transmitter and receiver PIC design. Owing to the high integration density of those PICs, interactions between components on the same chip in form of crosstalk, especially radio-frequency (RF) coupling, pose serious limitations and is the focus of this paper. At first, the generic foundry model is introduced in more detail and example designs of WDM transmitter chips are given. Afterwards, RF crosstalk issues are introduced and studied in experiment and simulation.

2. GENERIC PHOTONIC INTEGRATION

2.1. Generic Foundry Model

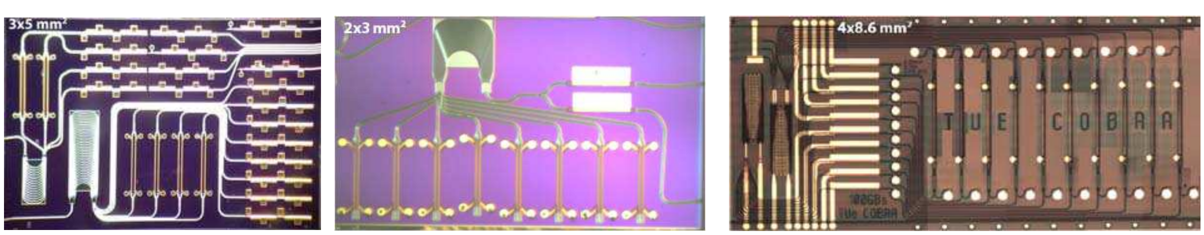
Although photonic integration density and complexity increased greatly through the years after its first emergence in the 1970s, its development did not experience such a fast pace as in case of microelectronics. The main reasons lies in the different methodologies followed in photonic and electronic integration. In photonics, most integration technologies are developed and optimized for one specific application, so that with time, the number of different technologies increased. Many of them are very similar to each other but still differ so much, that they cannot be easily transferred from one fab to the other. This lead to a fragmentation of integration processes, where no standard was available and each user had to spend effort and resources into application specific technology development first before having access to PICs. This is not the case in electronics, where a few standard processes are available (i.e., CMOS) that can serve a wide application and user group. Standard building-blocks (BBs) such as RLC-components, interconnects, diodes and transistors are defined with known performances from which complex circuits can be built up that suit the desired application. This approach can be also adopted for photonic integration because usually most of the PICs are made from a composition of basic BBs such as optical amplifiers, phase shifters, waveguides and couplers. From the basic BBs more complex composite BBs can be built to realized the different required functionalities in a PIC, leading to the definition of a generic photonic integration process.

The practical implementation of the generic integration processes is performed by fabs acting as foundries that offer multi-project wafer runs. Because the process is the same for all users and their applications, different designs can be collected on the same wafer and fabricated in the same run, allowing cost sharing by the users and a further reduction of chip cost. A process design kit (PDK) is provided by the foundries that facilitate the PIC design procedure through appropriate mask layout and simulation software. Essentially, the users of the foundry do not need to know about the process details but interact only with the PDK. This way, the generic foundry model to photonic integration can make low-cost PICs available to a broad range of users and has been adopted already by several industrial partners [3]. Readers are referred here to the literature for a more detailed treatment of this topic [4, 5].

2.2. WDM Transceiver PICs

Historically, PIC development has been driven by the demand for high-speed optical transmitter and receiver chips for telecommunications. Long-haul optical transport systems require high-quality lasers and high-speed modulators and detectors. By using integrated solutions instead of discrete components the transmission capacity and channel count could be easily scaled up, keeping a small footprint at the same time. The underlying costs of PIC development and fabrication were covered because they were destined for a high-performance market which tolerates expensive components. However, as optical technologies gain more attention in short-reach applications such as in access networks or for interconnects in data centers, low-cost devices are desired that can be produced in very large quantities and are widely accessible. Generic photonic integration plays a key role here, because it meets those requirements and can lead to circuits with very high performance. Some examples of WDM transmitter PICs are shown in Figure 1, all of which were fabricated from generic photonic integration processes. Figure 1(a) depicts a DBR-laser based PIC with an array of 8 lasers and 4 Mach-Zehnder modulators (MZM) operating above 10 Gbps from the Oclaro foundry [6]. Figure 1(b) shows an 8-channel reflective modulator chip from the same foundry based on Michelson interferometers for short-reach applications [7]. A 10-channel transmitter chip based on an AWG-laser and designed for aggregated 100 Gbps is shown in Figure 1(c) from the COBRA generic integration process.

As integration density and PIC complexity increases, many challenges emerge during the design of WDM transmitters. Due to the close spacing of components on the chip, undesired coupling effects in form of thermal, RF and optical crosstalk can occur in laser or modulator arrays. In particular, electric and magnetic field coupling between high-speed modulator electrodes is undesired and can lead to signal integrity issues. Furthermore, high-capacity transmitters have many electrical inputs and outputs that need to be addressed with a suitable packaging solution. All those issues and their impact on the chip performance need to be properly understood when scaling-out transmitter PIC complexity. Here, we focus on RF crosstalk effects in transmitter PICs.



(a) (b) (c)

Figure 1: (a) DBR based 4-channel WDM transmitter chip with Mach-Zehnder modulators [6]. (b) 8-channel WDM reflective transmitter chip based on Michelson modulators [7]. (c) AWG-laser based 10-channel transmitter.

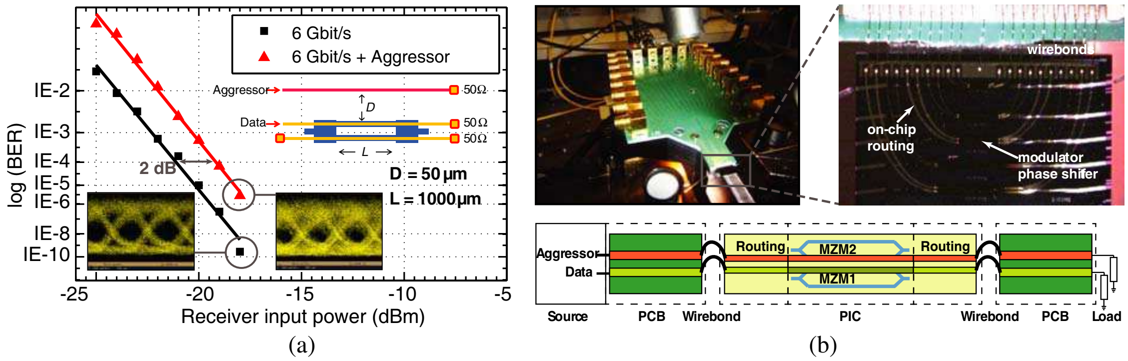


Figure 2: (a) Effect of RF crosstalk on BER curves measured on an assembly of modulator chip and high-speed PCB. (b) Several crosstalk sources contribute to the overall RF coupling in the assembly.

3. RF CROSSTALK IN PICS

3.1. Impact on System Performance

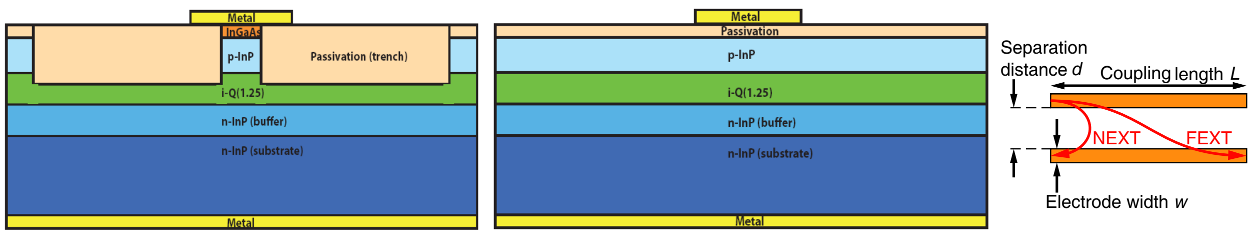
An example analysis of the impact of RF crosstalk on transmit system performance is presented to illustrate its importance. We have fabricated a test chip with closely spaced MZMs and on-chip electrical routing lines in the COBRA generic process as shown in Figure 2(b). The routing lines connect the travelling-wave phase shifters of the MZMs to bond-pads at the edge of the chip. A high-speed PCB is then connected to the chip through short wire-bonds for system-level measurements. To investigate any degrading effect of RF crosstalk, one channel is operated in single-drive mode with 50 Ω termination whereas a neighbour channel acts as an aggressor line. Overall crosstalk is then a combination of PCB, wire-bond, on-chip routing line and phase shifter crosstalk. Measured bit-error-rate curves with and without aggressor line are presented in Figure 2(a). It is evident that a 2 dB power penalty is introduced here due to the effects of RF crosstalk. Noise caused by the aggressor degrades the optical eye diagram at 6 Gbps visibly which leads to the observed power penalty.

The results indicate that RF crosstalk can have a significant effect on PIC system performance. However, it is very difficult to relate the effect of crosstalk specifically to one of its many possible sources. Usually, crosstalk in electronic packages such as in PCBs can be controlled properly with given effort and techniques in PCB design. This is more difficult for wire-bond interfaces to the PIC but crosstalk could be essentially reduced using alternative technologies such as flip-chip bonding. However, RF coupling on the PIC itself has not been investigated much so far as it only recently became important with high channel-count PICs with close channel spacing and high integration density emerged. One possibe way to analyze RF crosstalk within the PIC is presented in the following.

3.2. Crosstalk Simulations

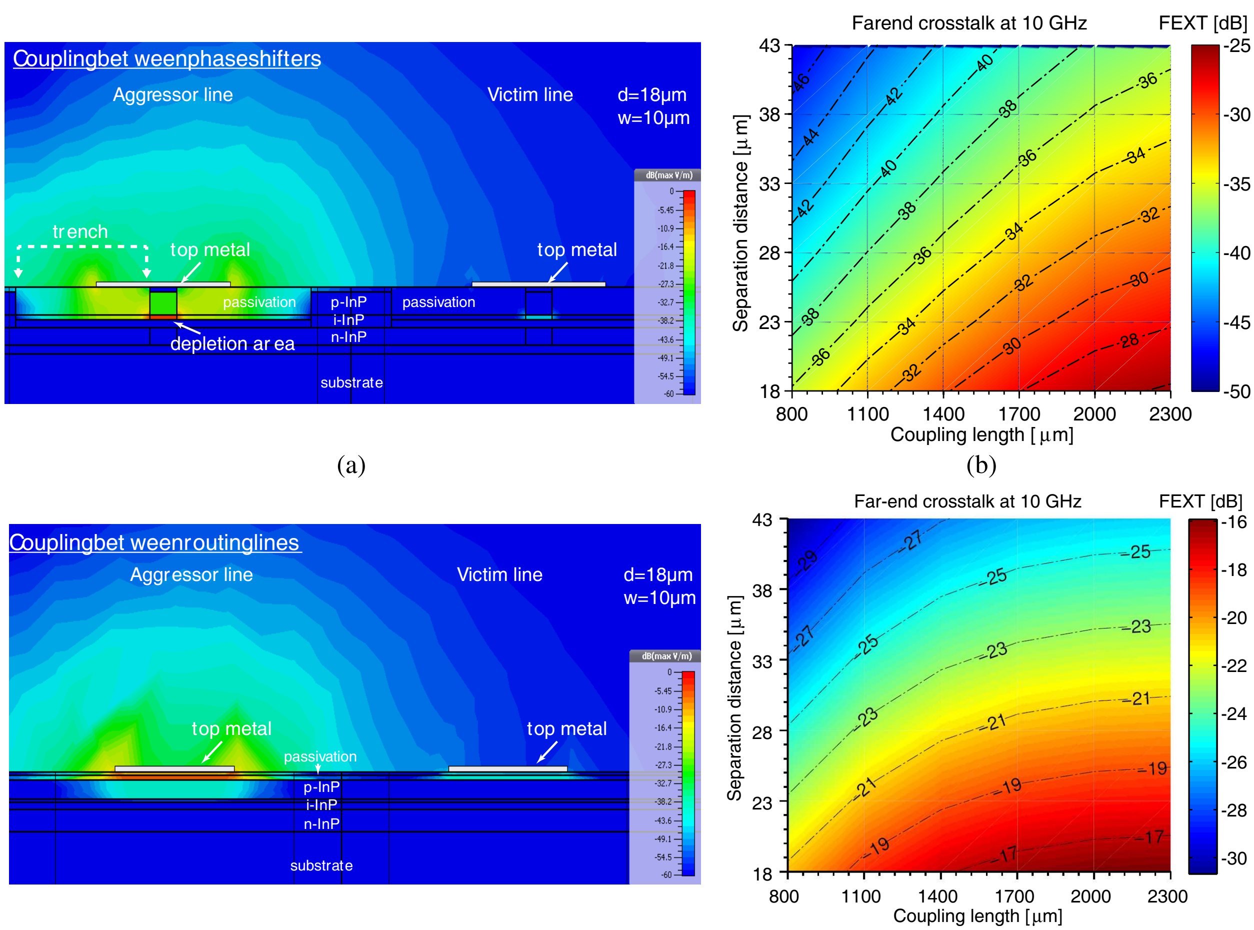
To continue the example above, crosstalk between on-chip routing lines and electro-optical phase shifters from the COBRA generic integration process is analyzed using the commercial 3D field solver CST MWS. It has been shown in the literature that FEM and FDTD based field solvers are able to accurately simulate the microwave behaviour of electro-optical phase shifters [9, 10]. The method has been used before to model electrical properties of single phase shifters from the COBRA integration process [11] and is extended here to account for crosstalk effects of two coupled phase shifters and routing lines.

Figures 3(a) and 3(b) show the layer build-up of the phase shifter and routing line respectively which are both metal-insulator-semiconductor transmission lines. When two transmission lines are coupled together, we distinguish between near-end (NEXT) and far-end crosstalk (FEXT) as illustrated in Figure 3(c). In the first approximation, FEXT is more important for the modulation process, as it co-propagates with the optical signal, and accordingly we can restrict ourselves to FEXT in the following. To have a better understanding of the coupling process, electric field plots of two closely spaced phase shifters and routing lines are given in Figures 4(a) and 4(c). We can make out distinct differences between the two with respect to field concentration and coupling. In the former, the field is concentrated close to the depletion area of the optical waveguide, because the top metal is electrically connected to the doped semiconductor underneath through a highly doped contact layer. In the latter case, the field takes the form of a typical microstrip line, localized within the passivation layer directly below the top metal. This leads to different coupling of the electric field. For the phase shifters, most of the evanescent field is kept within the trench region, because the semiconductor stack in the middle between the two phase shifters acts as a shield, so that only a small amount couples from the aggressor to the victim line through air. For the routing lines however, no such trench exists and coupling occurs through the passivation layer and air, not shielded by the semiconductor stack below, and more field arrives at the victim line. Magnetic field coupling (not shown here) is not affected by the trench and also contributes to the overall FEXT. Figures 4(b) and 4(d) show the overall FEXT for varying coupling distances and lengths at 10 GHz in case of phase shifters and feeding lines respectively. In general, reducing the separation distance or increasing the coupling length will increase FEXT. The dependence on the coupling length starts



(a) (b) (c)

Figure 3: (a) Cross-section of high-speed electro-optical phase shifter and (b) cross-section of on-chip RF routing line from the COBRA generic integration process. (c) Illustration of two coupled lines.



(a) (b) (c) (d)

Figure 4: (a) Electric field coupling between MZM phase shifters ($w = 10\,\mu\text{m}$, $f = 14\,\text{GHz}$) and their FEXT variation (b) depending on coupling distance d and length L. (c) Electric field coupling between on-chip routing lines ($w = 10\,\mu\text{m}$, $f = 14\,\text{GHz}$) and their FEXT dependence on coupling geometry.

to saturate after a certain value because the coupling mechanism resembles that of a directional coupler and shows periodicity in frequency and coupling length. When comparing Figures 4(b) with 4(d), coupled routing lines experience more than 10 dB higher FEXT than coupled phase shifters for the same geometry, which can be attributed to the effect of the trenches mentioned earlier. Crosstalk can be kept below −30 dB for usual modulator length of 1.5 mm when placing phase shifters more than 20 µm away from each other, whereas 1 mm long routing lines need at least 40 µm spacing to achieve comparable low crosstalk levels.

It has been shown through simulations that routing lines contribute more to crosstalk effects on the PIC than modulator phase shifters, which is a useful insight for PIC design. Furthermore, using this methodology, design rules can be defined for determining minimum distances between components to avoid excessive crosstalk. Additionally, 4-port matrix representations can be extracted and used in circuit level analysis and simulation.

4. CONCLUSION

This paper has reviewed the basic ideas of generic photonic integration and outlined how it can speed up PIC complexity development and reduce its costs. Examples of WDM transmitter PICs based on this approach were given and in a test chip from the COBRA process, RF crosstalk, leading to 2 dB power penalty, has been identified as a major impairment for such systems. A 3D-solver based simulation model has shown that on-chip routing lines generate higher crosstalk than modulator phase shifters. The presented simulation methodology can be used to introduce design rules for crosstalk minimization and used together with circuit-level based simulations for RF design in transmitter PICs. Further experimental verification and estimation of the amount of tolerable crosstalk level need to be performed in future.

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