An Ultra-wideband and Low Phase Noise LC-VCO Using NMOS Varactor with MOM Digital Capacitor Switching Arrays

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Abstract— This paper presents a novel low-phase-noise and ultra-bandwidth LC-tank voltage-controlled oscillator (VCO). The work fully-integrated 5.8 GHz VCO designed and simulated using 130-nm CMOS technology. Instead of using the conventional varactor in the tank design, a novel metal-oxidemetal (MOM) digital capacitor switching array (MOMDCSA) has been implemented with nMOS varactor is employed as an effective varactor bank. The proposed VCO-measured results at the centre frequency demonstrate a phase noise of −129.7 dBc/Hz and FOM of −198.38 dBc/Hz at 1 MHz frequency offset. The VCO shows approximately 33% tuning range under a power consumption of 2.8 mW.

1. INTRODUCTION

The recent exponential growth in higher integration and wireless communication has attracted tremendous effort to develop more channels in mobile communication applications [1]. VCOs are considered to be one of the important parameters in analogue and digital systems. Nowadays, the demand for high-performance, VCOs is increased; in turn, this demand has imposed more strict requirements on the phase noise of the VCO [2].

The phase noise of the VCO is used to describe phase fluctuations due to the random frequency fluctuations of a signal. Phase noise can be caused by a number of conditions, but is mostly affected by VCO frequency stability. It is one of the most important parameters for the quality and performance of information transfer, in turn affecting the reliability purposes in data communication. VCOs are a major design challenge and thus have received a lot of attention in recent years. Spectacular works considering switching capacitances inside the LC-tank have been conducted to extend the tuning range and improve the phase noise of VCO's [4–6]. However, these switches were implemented using stacked devices and a large size resistors to gain high impedance for RF signals and this occupied a larger die area. In addition, the dissipation power is relatively high and the measured and the simulated phase noise are still high.

This article, introduce a high performance 3-bit MOMDCSA using (MOM) digital switching capacitors for coarse tuning and body-grounded NMOS varactors for fine tuning in order to keep the VCO gain (Kvco) and variation low, to extend the bandwidth and minimize phase noise variance through the whole tuning range at the cost of chip size. The structure uses an adequate metal-oxide-metal (MOM) capacitors taking advantage of their high capacitance density, low parasitic capacitance and thinner dielectric. The proposed structure solves the conflict of high phase noise variation due to wider tuning range, minimize the sensitivity of the VCO noise by optimizing the gain and has an output frequency which varies linearly with control voltage. This paper is organized as follows: Section 2 explains the VCO's core design and the implementation process, while Section 3 presents the simulation results, followed by the conclusion in Section 4.

2. CIRCUIT DESIGN AND IMPLEMENTATION PROCESS

Cross-coupled NMOS differential VCO based on binary weighted switched capacitor bank ad body-grounded nMOS varactor is depicted in Fig. 1. The LC tank is consists of a differentially tuned varactor a very small size symmetrical center-tapped inductor, the metal width and the lateral spacing between them were optimized to improve and to obtain an appropriate parasitic capacitance and a high Q, the measured quality factor Q was 16.50, for 460 pH inductors while the area was 16596 μm^2. The cross connected differential pair provides the negative resistance to neutralize the tank losses with less current consumption and hence is more power efficient.

The wider varactors bandwidth the higher phase noise [3], RF VCO with sub-bands is the best choice for broadband implementation. The key contribution of this work is to design a broadband VCO employing the MOMDCSA to lower KVCO and improve tuning linearity and obtains a minimum phase noise variation within all tuning ranges. The total tank capacitance is established

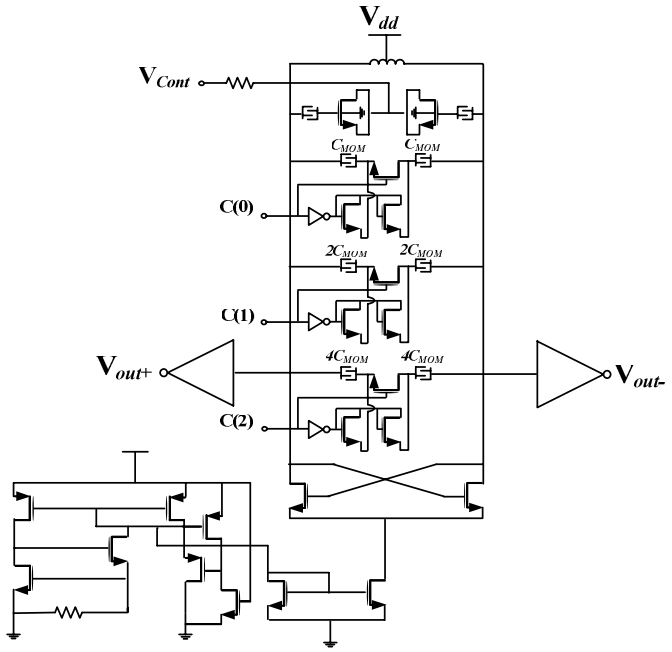

Figure 1: Schematic diagram of the designed 5.8 GHz 130 nm CMOS VCO.

by the nMOS varactor and the fixed MOM capacitance due to the parasitic and the switched MOM capacitance. MOS-based varactors are commonly used in VCOs due to their wider tuning range and higher Q factor [3], and lower phase noise. The nMOS varactors may have an advantages over pMOS varactors by its asymmetric characteristics effectiveness of area, which result less power consumption. In addition, the maximum capacitance per unit of area is approximately three times higher than that of a PN-junction varactor [1].

3. SIMULATION RESULTS

The proposed VCO was implemented using a commercially available UMC-130 nm, 6-metal, mixed mode CMOS process and simulated using Cadence Virtuoso Analogue Design Environment Tools. Simulation results indicate that the VCO exhibits wider tuning range from 4.84 GHz to 6.76 GHz and FoM varies from −201.7 dBc/Hz to −204.9 dBc/Hz as shown in Fig. 2.

The gain variation of the VCO has been reduced to 13.95%. As a result, the VCO immunity increases and the possibility of false locking for instant in PLL applications will decrease. In addition, the new varactor achieves steep transition for tuning voltages as depicted in Fig. 2. The circuit generates stable periodic signals with a harmonic index and measured output power of 3.73 dBm at the resonance frequency, as shown in Fig. 3, with tuning voltage varying from 0 to

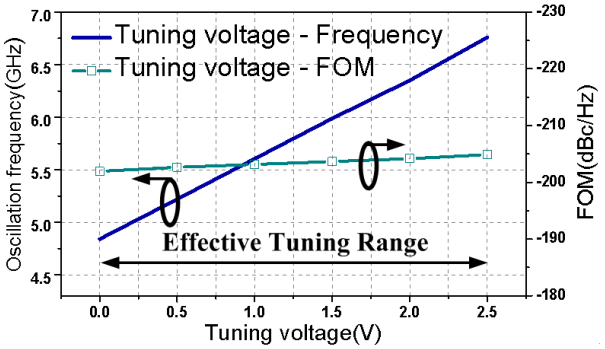

Figure 2: Tuning characteristics and FoM of the VCO.

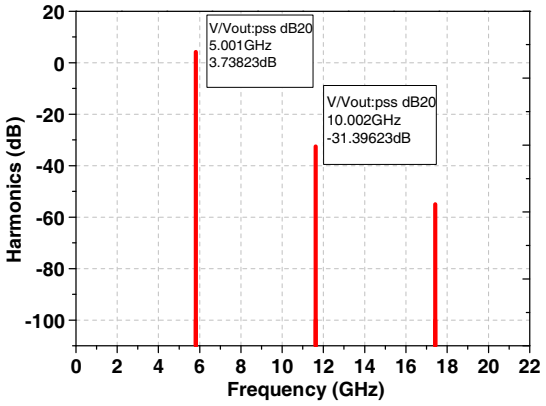

Figure 3: Simulated power output plot of a 5.8 GHz VCO.

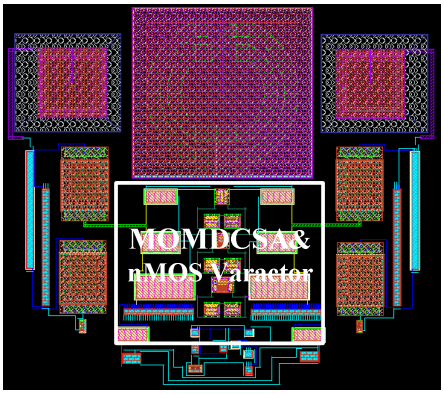

Figure 4: Layout of the designed CMOS VCO.

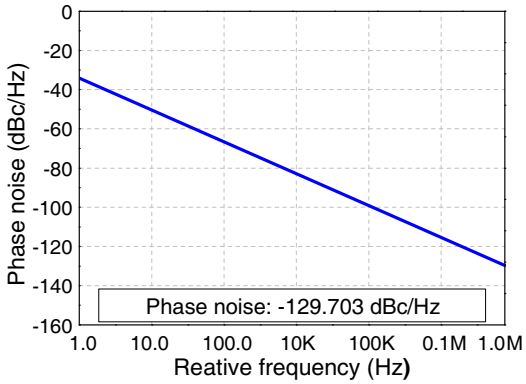

Figure 5: Simulated phase noise at 1 MHz offset.

3.0 V. The phase noise of an LCVCO is described, according to Leeson [3], as:

$$L\left(f_m\right) = 10\log\left[\frac{1}{2}\left(\left(\frac{f_0}{2Q_l f_m}\right)^2 + 1\right)\left(\frac{f_c}{f_m} + 1\right)\left(\frac{FKT}{P_s}\right)\right] \tag{1}$$

Figure 4 shows the layout of the proposed VCO, the core circuit, and the output buffer occupies a silicon area of $862 \times 986\ \mu m^2$ not including the bond pad. Circuit performance, which was simulated using cadence to show the transient analysis of the VCO, demonstrates clearly that steady-state oscillation starts at approximately 6.27 ns.

The results obtained from the simulation of the LC-VCO design show that the phase noise has been drastically reduced. A brief description of the performance summary is illustrated in Table 1. The phase noise is automatically decreased while the power consumption is reduced. Thus, there is a trade-off between the power consumption and phase noise [1]. The phase noise of −129.7 dBc/Hz at 1 MHz frequency offset as shown in Fig. 5.

Table 1: Performance comparison of CMOS VCOs.

Process	F (GHz)	P (mW)	PN (dBc/Hz)	Offset	TR (GHz)	FoM (dBc/Hz)	Ref.
0.18 µm CMOS	5.00	7.20	−90.20	1.0	4.10–5.00	−154.80	[4]
0.18 µm CMOS	4.20	4.50	−119.0	1.0	4.10–4.80	−184.47	[5]^S
0.18 µm CMOS	5.00	13.00	−121.5	1.0	5.10–5.36	−192.10	[6]^S
0.18 µm CMOS	5.20	9.70	−113.7	1.0	4.39–5.26	−180.00	[8]
0.18 µm CMOS	5.80	10.08	−117.0	1.0	5.27–6.41	−184.00	[9]
0.13 µm CMOS	5.80	2.88	−132.7	1.0	4.84–6.76	−198.38	This work^S

F: Centre frequency, P: power, PN: Phase noise at 1 MHz, * at 10 MHz offset, TR: Tuning range, FoM: Figure of Merit, S: Simulation.

To compare the performance of previously published oscillators, and FOM, the one we have used was adopted by Ham and Hajimiri [7], and it normalizes the measured phase noise with respect to center frequency and power consumption. It is defined by Equation (2):

$$\text{FOM} = L\left\{\Delta f\right\} - 20\log\left\{\frac{f_0}{\Delta f}\right\} + 10\log\left\{\frac{Pd}{1\,\text{mW}}\right\} \tag{2}$$

A brief description of the performance summary and comparison with published work has been mentioned in Table 1, and shows that the design of the proposed VCO proved to be state of the art. The phase noise is considerably good where the FOM is found to be excellent.

4. CONCLUSION

We demonstrated a 5.80 GHz low-phase-noise and low-power LC-VCO based on cross-coupled topology using a 130 nm CMOS technology. We can conclude that the proposed MOMDCSA and the

nMOS varactor have better characterizations than other switches and a more significant effect on the reduction of phase noise. The feasibility of a high-performance, high-frequency VCO is demonstrated. The phase noise of the oscillator was optimized and the measured worst-case phase noise is −129.7 dBc/Hz at 1 MHz frequency offset. As a result, this CMOS VCO achieves the best FOM of −198.38 dB. The VCO shows approximately 33% tuning range and consumes 2.8 mW from a 3.3 V power supply.

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