Digital Multi-channel High Resolution Phase Locked Loop under Influence of Potential System Uncertainties

Mohamed Rizk, Shawky Shaaban, Usama Aboul-Nadar, and Alaa El-Din Sayed Hafez
Alexandria University, Alexandria, Egypt

Abstract— This paper is devoted to present a multi-channel, high resolution, fast lock phase locked loop (PLL) for surveillance radar applications under influence of system noise. Phase detector based PLLs are simple to design, suffer no systematic phase error, and can run at the highest speed. Reducing loop gain can proportionally improve jitter performance, but also reduces locking time and pull-in range. The system is studied under influence of system noise in the range from 5 to 30 dB to reflect the reliability of the system under these conditions. The results perform a comparison of noise power, VCO control input, Lock time, ISE and ITSE Performance indices for three selective channels among 38 channels operated in the desired frequency range. The results show superiority of the system in difficult operating conditions.

1. INTRODUCTION

Phase-locked loops (PLLs) are used in surveillance radar wave formers to implement a radar waveform synthesis. The major concerns in the design of PLLs are noise or jitter performance and the lock time. G. David [1], describe two simply implemented frequency detectors which, when added to the traditional phase detector, can improve acquisition even for very small loop bandwidths and large initial frequency offsets. Kurt M. Ware et al. [2] presents a numerical system simulation program that explores the time-domain behaviour of an idealized model based on the phase-locked loop design. Faster lock is attained while maintaining the PLL's gain/phase margin characteristics by B. David et al. [3]. Kent Kundert [4], presents a methodology for predicting the jitter performance of a PLL using simulation. Several researches introduce an improvement for the jitter and frequency lock time [5–11] but not consider multi-channel, high resolution PLLs Digital phase-locked loop (DPLL) design one of most active research topics in complex digital communication systems. It replaces traditional PLL designs, a charge-pump and voltage controlled oscillator (VCO) [12]. A new method for tracking narrowband signals acquired via compressive sensing is designed in Ref. [13]. This paper presents a multi-channel, high resolution PLL for surveillance radar systems based on developing the charge pump by a digital adaptive gain processor to achieve fast lock times while improving jitter performance in lock. Section 2 provides a theoretical analysis of the frequency synthesis and the phase locked loop. Section 3 briefly describes the proposed PLL architecture. Section 4 introduces a discussion about potential system uncertainties. Definition of the performance indices introduced in Section 5. Section 6 discusses the results and a summary is in Section 7.

2. THEORETICAL DESCRIPTION

The PLL is a well-established method for tracking the frequency and phase of a signal $\mathbf{s(t)}$ using a feedback loop to continuously update an estimate of the signal. Figure 1 shows a general PLL architecture. In general, phase locking uses three component operations as generically depicted below,

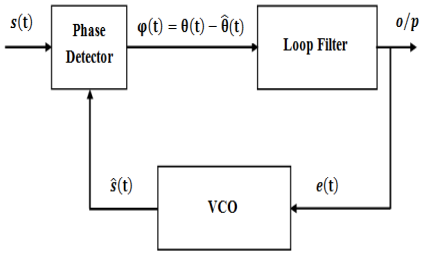

Figure 1: General phase locked loop architecture.

Phase-error generation — this operation, sometimes also called "phase detection," derives a phase difference between the received signal's phase $\boldsymbol{\theta}(\mathbf{t})$ and the receiver estimate of this phase, $\hat{\boldsymbol{\theta}}(t)$. The actual signals are [14],

$$s(t) = \cos(\omega_{to} + \theta(t)) \tag{1}$$

and

$$\hat{s}(t) = \cos\left(\omega_{to} + \hat{\theta}(t)\right) \tag{2}$$

but only their phase difference is of interest in synchronization. This difference is often called the phase error,

$$\square(t) = \theta(t) - \hat{\theta}(t) \tag{3}$$

3. THE PROPOSED PLL ARCHITECTURE

The proposed PLL synthesize 51 frequency channels from 1.250 to 1350 MHz with frequency separation of 2 MHz the general architecture of the proposed digital PLL is demonstrated in Figure 2. The synthesized frequency is divided by 625 to 675 corresponds to 51 frequency channel to produce 20 MHz signal compared with 20 MHz reference signal via XOR operation. The error signal from the comparator will be filtered with cut-off frequency of 100 kHz. The Butterworth filter is the best compromise between attenuation and phase response. It has no ripple in the pass band or the stop band, and because of this is sometimes called a maximally flat filter as shown in Figure 3. The output from the filter is converted to digital format in order to adaptively scale the error signal through adaptive digital multiplier. The block diagram of the designed digital compensator is shown in Figure 4. The digital multiplier scale the input signal according to the channel frequency code according to the following formula,

$$V(f) = U(f) * (\alpha N + \beta) \tag{4}$$

where $U(f)$ is the LPF output, α, β constants equal to 0.038, -17.75 respectively, N is the frequency division ratio of the selected operation frequency.

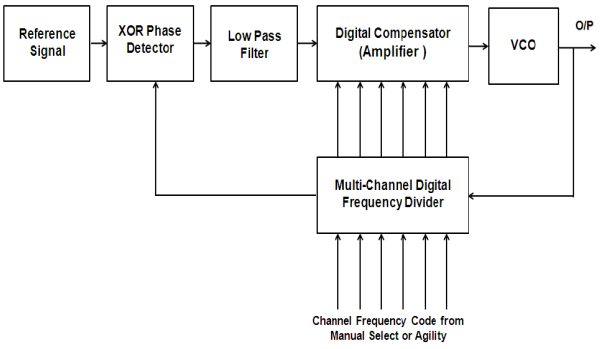

Figure 2: General architecture of the proposed PLL.

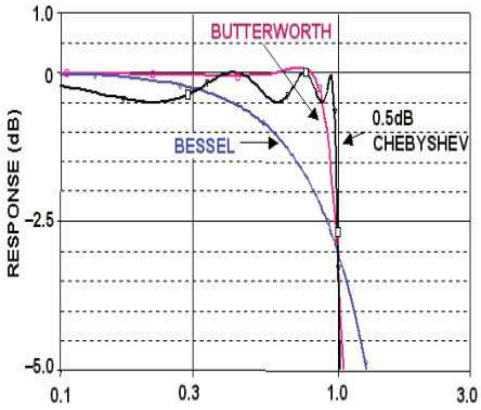

Figure 3: Comparison of amplitude response of Bessel, Butterworth, and Chebyshev filters.

4. POTENTIAL SYSTEM UNCERTAINTIES

A control system design assumes knowledge of the model of the plant and controller and constant parameters. The plant model will always be an inaccurate representation of the actual physical system because of parameter changes, unmodeled dynamics, sensor noise, and unpredicted disturbance inputs. The goal of robust systems design is to retain assurance of system performance in spite of model inaccuracies and changes. A system is robust when the system has acceptable changes in performance due to model changes or inaccuracies [16, 17]. The system structure that incorporates potential system uncertainties is shown in Figure (5). This model includes the sensor

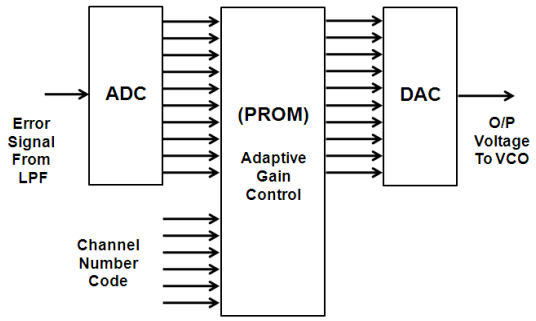

Figure 4: Digital compensator block diagram.

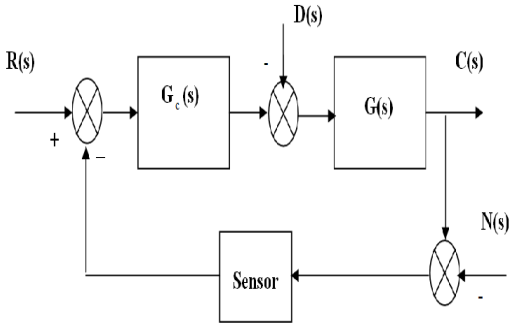

Figure 5: Closed-loop structural diagram.

noise $N(s)$, the unpredicted disturbance input $D(s)$, and a plant $G(s)$ with potentially unmodeled dynamics or parameter changes. The unmodeled dynamics and parameter changes may be significant or very large, and for these systems, the challenge is to design a system that retains the desired performance.

5. PERFORMANCE INDICES

Increasing emphasis on the mathematical formulation and measurement of control system performance can be found in the recent literature on automatic control. Modern control theory assumes that the systems engineer can specify quantitatively the required system performance. Then a performance index can be calculated or measured and used to evaluate the system's performance. A quantitative measure of performance of a system is necessary for automatic parameter optimization of a control system, and for the design of optimum systems [18, 19]. Whether the aim is to improve the design of a system or to design a control system, a performance index must be chosen and measured. A performance index is a quantitative measures of the performance of a system chosen so that emphases, is given to the important system specifications. A system is considered an optimum control system when the system parameters are adjusted so that the index reaches an extreme value, commonly a minimum value. A performance index, to be useful, must be a number that is always positive or zero. Then the best system is defined as the system that minimizes this index. A Suitable performance index is the integral of the square of the error, ISE, which is defined as:

$$\text{ISE} = \int_0^T e^2(t)dt \tag{5}$$

The upper limit T is the finite time chosen somewhat arbitrarily so that the integral approaches a steady-state value. It is usually convenient to choose T as the settling time, This performance index is designated the integral of the time multiplied by absolute error, ITAE. Another similar index is the integral of time multiplied by the squared error, ITSE:

$$\text{ITSE} = \int_0^T te^2(t)dt \tag{6}$$

A control system is optimum when the selected performance index is minimized. However, the optimum value of the parameters depends directly on the definition of optimum, that is, the performance index.

6. RESULTS

The proposed architecture is simulated using Matlab program Simulink. Next, we evaluate the effectiveness of the proposed technique. We assume that the frequency channels changes dynamically from Channel 1 to channel 51 with fixed and adaptive gain for comparison purpose. Figure 6 shows the transient time for the control signals which feed to the VCO in case of three selected channels for example. It is clear from the figure that it is no overshot, all the channel are stable and reach the desired frequency value, and the lock times of the desired channels are between 7 µsec

for the first channel and 11.5 µsec for the last channel. The simulation block diagram is shown in Figure 7. The system is studied under influence of system noise in the range from 5 to 30 dB to reflect the reliability of the system under these conditions. The system uncertainties are simulated as a Wight noise added to the control signal as shown in Figure 8. The noise power has considered

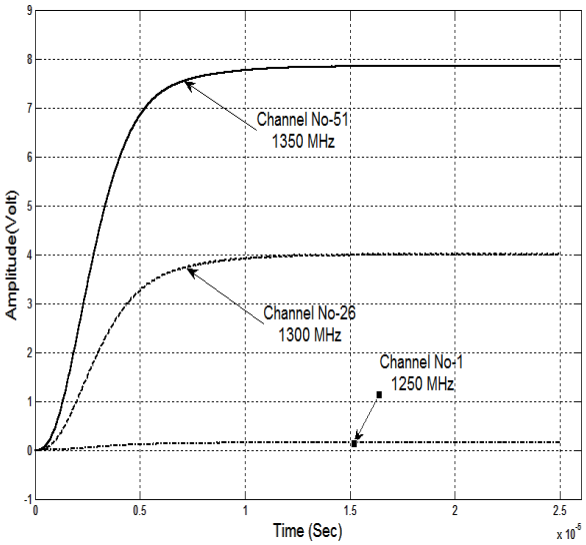

Figure 6: Control action transient.

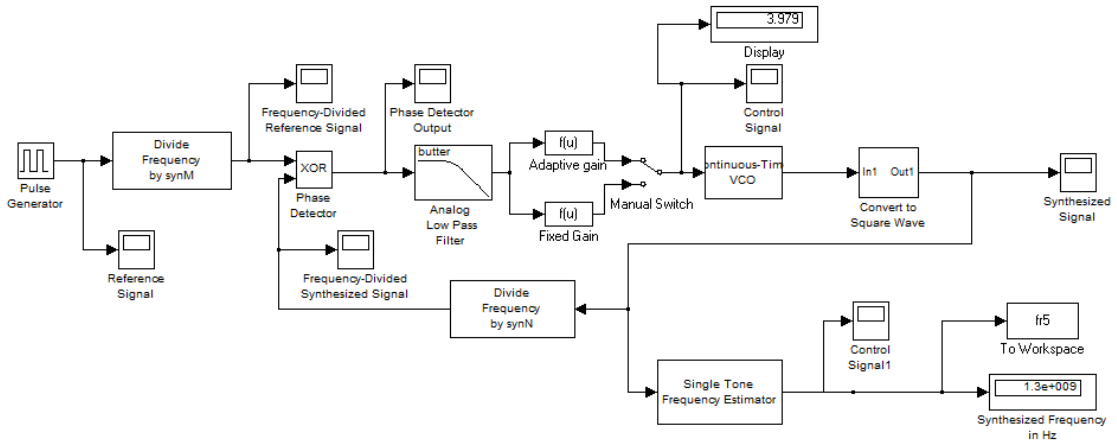

Figure 7: PLL Simulink block diagram.

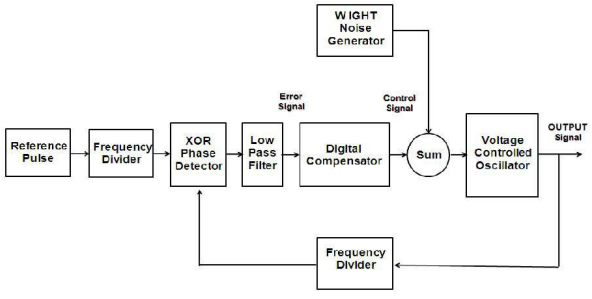

Figure 8: PLL with uncertainties.

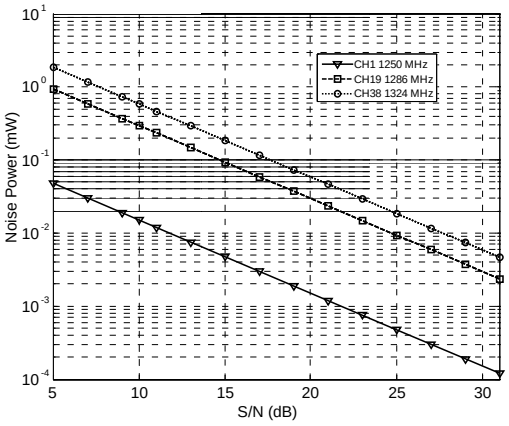

Figure 9: Noise Power versus S/N for three channels.

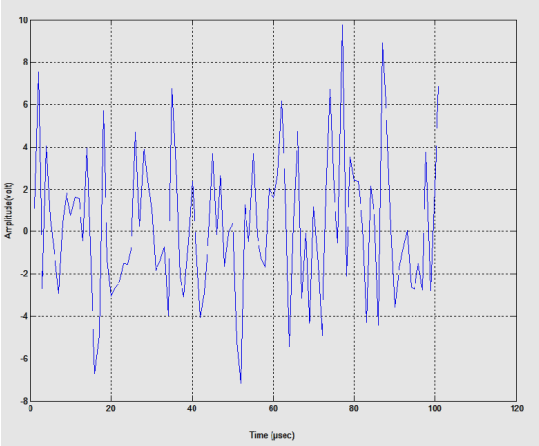

Figure 10: Shape of Wight noise.

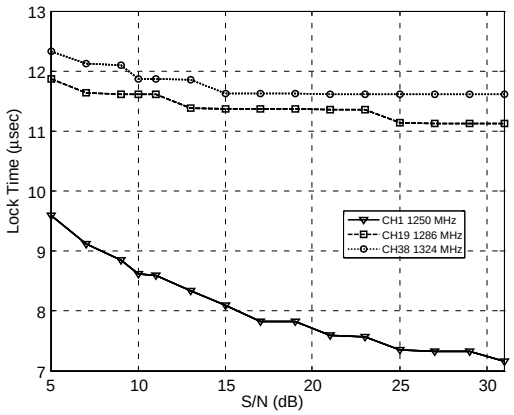

Figure 11: Lock time versus S/N for three channels.

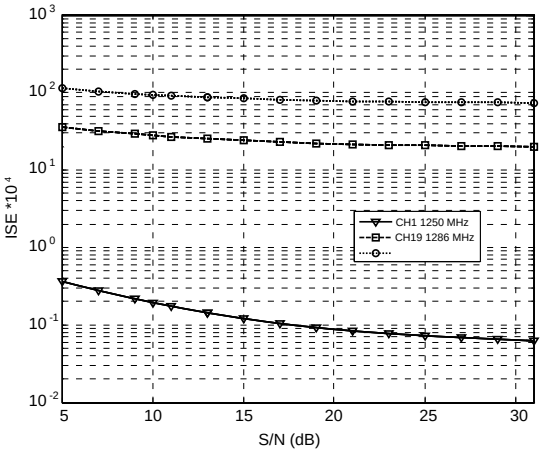

Figure 12: ISE index versus S/N for three channels.

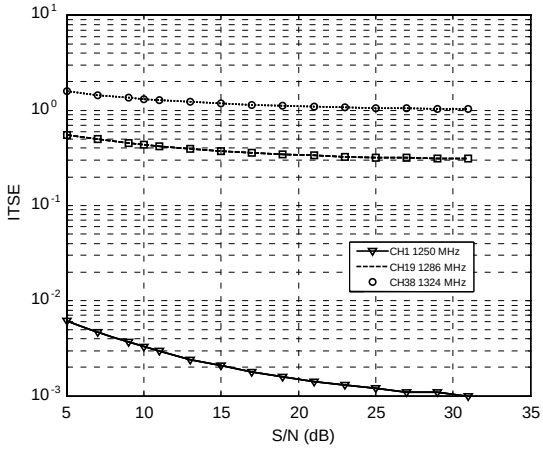

Figure 13: ITSE index versus S/N for three channels.

value corresponding to S/N ratio as shown in Figure 9 for three selected channels. When the noise showed in Figure 10 is added to the control signal, only the first 38 channels are completely stable and have a lock time 9.58 μsec for the first channel, and lock time 12.325 μsec for the last channel as shown in Figure 11. The proposed system is considered an optimum control system when the system parameters are adjusted so that the performance index reaches a minimum value. The two performance index ISE, and ITSE which discussed in Section 5, are used to test the optimality of the system under influence of system noise. Figures 12, 13 show that the performance indices is decreased when the S/N ratio increase.

7. CONCLUSION

This paper presents a multi-channel, high resolution PLL for surveillance radar systems based on developing the charge pump by a digital adaptive gain processor to achieve fast lock times while improving jitter performance in lock. The design also improves the frequency agility capability of the radar system. The results show a fast lock, high resolution PLL with transient time less than 12.325 μsec which is suitable for radar applications. The proposed system is tested under influence of system noise in the range from 5 to 30 dB. The results show superiority of the system in difficult operating conditions.

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