Design of Broadband Vector Modulator Based on HMC500LP3 Chip

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Abstract— Vector modulator technology in active phased array antenna has been used as a replacement of conventional digital phase shifter and digital attenuator. In this paper, vector modulator is realized by a vector modulation HMC500LP3 chip from Hittite company using Agilent ADS software. The HMC500LP3 is a Vector Modulator RFIC with high dynamic range and differential input. As a demonstration of the vector modulator's flexibility, the HMC500LP3 chip has been fabricated and characterized by means of S-parameter measurements. What's more, this paper systematically presents the vector modulator measurement step which uses Agilent USB/GPIB control module 82357B to have logic control of vector network analyzer and DC Power Analyzer by MATLAB software. The DEEMBDING calculation for SMA connector is completed by the MATLAB software. Finally, the measurement results show that the chip of the HMC500LP3 vector modulator can realize a continuously controlled 360° phase shifting range and a range of (−9 dB)–(−41 dB) for the amplitude over the 1.8 GHz–2.2 GHz band. Measured S_{11} and S_{22} are below −17 dB and −15 dB.

1. INTRODUCTION

Active phased array antenna system has recently attracted considerable interest in the antenna technology research. The problem of improving the precision of phase shifting has not been addressed until M.Tuckman proposed the concept module of the vector modulator in 1988 [1]. The complexity of designing a digital phase shifter increases with the operating frequency and poor uniformity of digital attenuators, while the application of vector modulator can largely decrease hardware complexity, reduce the size of the component, lower cost, and improve the flexibility of amplitude modulation and phase modulation [2].

Figure 1 shows the schematic and principle of the vector modulator presented. A 3-dB Lange coupler splits the input signal into two orthogonal portions: in-phase and quadrature-phase. These two portions are attenuated by two bi-phase amplitude modulators, which are controlled by two bias voltages I and Q respectively. Combining these two modulated portions with a Wilkinson coupler completes the modulating function [3].

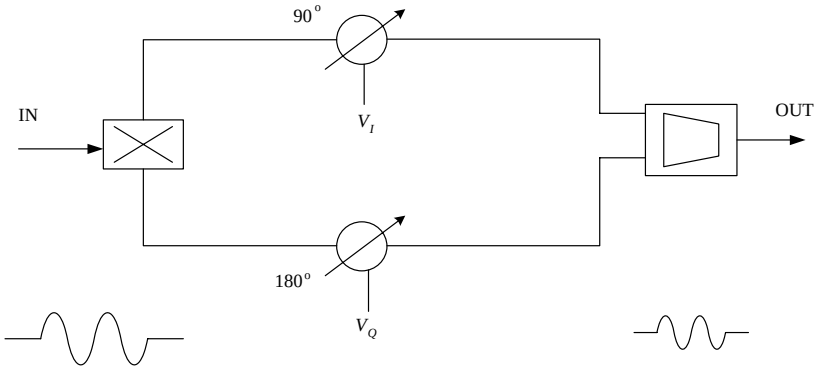

Figure 1: Typical schematic diagram of the vector modulator.

2. CIRCUIT DESIGN

2.1. Features of the HMC500LP3 Chip

Figure 2 shows the schematic of the HMC500LP3 chip. According to the datasheet, I & Q ports of the HMC500LP3 can be used to continuously vary the phase and amplitude of RF signals by up to 360 degrees and 40 dB respectively. The chip supports a 3 dB modulation bandwidth of 150 MHz. The input IP3/noise floor ratio is 185 dB with an input IP3 of +33 dBm and input noise floor of −152 dBm/Hz. These parameters can meet the demand of the vector modulator design.

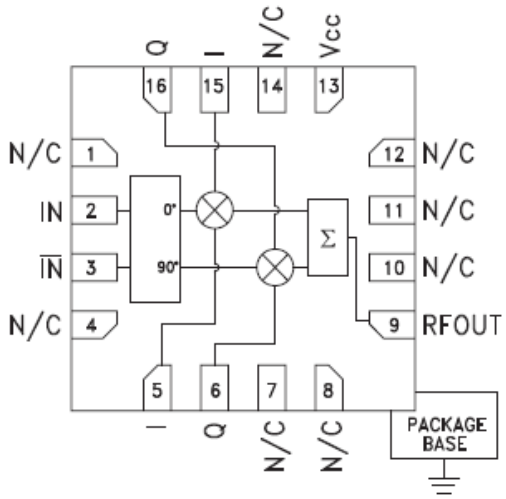

Figure 2: Schematic of the HMC500LP3.

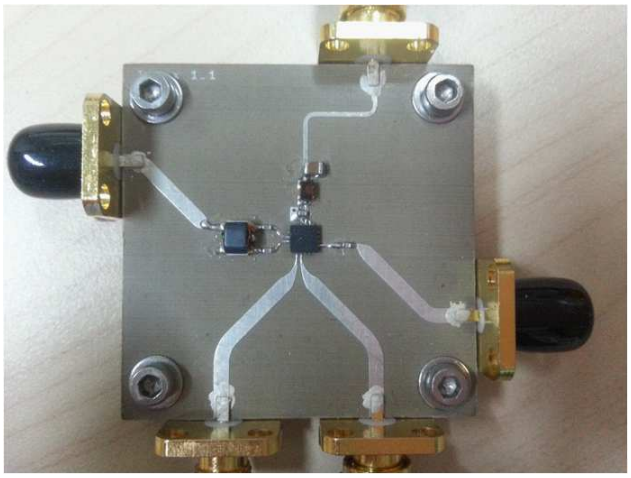

Figure 3: A photograph of HMC500LP3.

A photograph of the vector modulator chip and its peripheral circuit is shown in Figure 3. The chip is bonded on a test substrate. The required chip area is only 4 cm × 4 cm.

The thickness of the board is confirmed to 30 mil based on the TC350 substrate. According to the properties of the board, the width of 50 ohm microstrip line is 1.6712 mm calculated by the ADS software. For optimum performance, the input should be AC coupled and driven through a Balun BD1631J50100AF with an approximately 100 Ω differential impedance. Similarly, the output should be DC blocked.

The I-Q input promises to be a vital component for the realization of vector modulator, with pin 5 chosen as I voltage input pin 6 as Q voltage input. For the feed circuit, the nominal voltage supply for the HMC500LP3 is 7.6 V and is applied to the pin 13. All the pins are gradually connected so that reflection and parasitic capacitance can be reduced. Because the power supply circuit noise at the work frequency may have a bad effect on the chip, each of the supply pins is connected with a capacitor in 0402 package and a inductor in 0805 package to provide high frequency bypass near the operating frequency.

Solder The exposed paddle on the underside of the package is soldered to a low thermal and electrical ground plane. These layers should be stitched together with 5 vias under the exposed paddle, because the rise of the chip's temperature can lead to the decrease of chip life, even make the chip burned down.

3. PRODURES OF THE TESTING

Taking precision and verifiability into consideration, closed loop calibration method is adopted in this paper. Figure 4 and Table 1 show the general characterization bench setups used extensively for the HMC500LP3. The whole system is composed of vector network analyzer, DC power analyzer and control computer with each instrument being connected by GPIB Bus. An automated VISA program is used to control the R&S ZVA24 vector network analyzer and the Agilent DC power analyzer model N6705 is connected by GPIB. DC power analyzer can provide 3 independent voltage and current outputs, so we set CH1 for the vector modulator module power supply channels and CH2/CH3 for in phase/orthogonal control signal respectively.

Table 1: Input return loss vs I voltage and Q voltage.

DC power analyzer model N6705	CH1 for network analyzer
	CH2 for in phase control signals
	CH3 for orthogonal control signal
R&S ZVA24 Vector network analyzer	Measure HMC500LP3 S parameters
GPIB Address	5: DC power analyzer N6705 20: Vector network analyzer

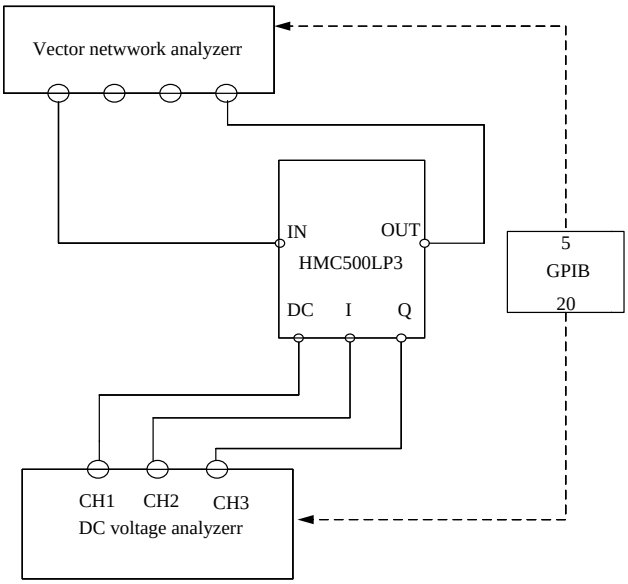

Figure 4: S parameter measurement setup.

After insuring the instrument having been installed well, we set 0 V as the initial value of power supply module and increase it through three different ways: from 0 V to 1 V at intervals of 0.1 V, from 1 to 7 V at intervals of 0.5 V, from 7 V to 7.4 V at intervals of 0.1 V. I control voltage is increased from 0 V to 0.5 V at intervals of 0.1 V, the same as Q control voltage.

Five different voltage values, 7.5 V, 7.75 V, 8 V, 8.25 V, 8.5 V, are set up in the DC voltage supply. Under the different DC voltage supply, I/Q control voltage are respectively set up 11 points which is swept from 0.5 V to 2.5 V at the intervals of 0.2 V. S-parameters are measured under the above

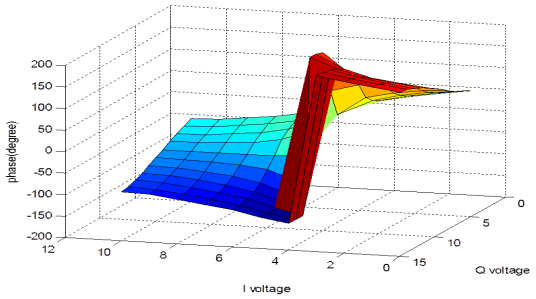

Figure 5: Phase vs I/Q voltage at the 7.75 V DC su]

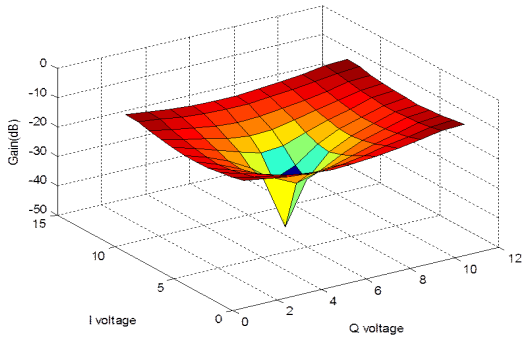

Figure 6: Gain vs I/Q voltage at the 7.7 5V DC su]

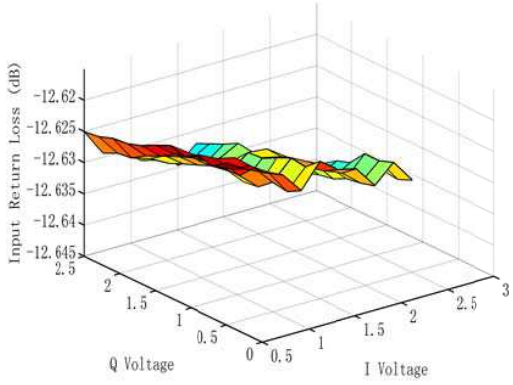

Figure 7: Input return loss vs I voltage and Q voltage.

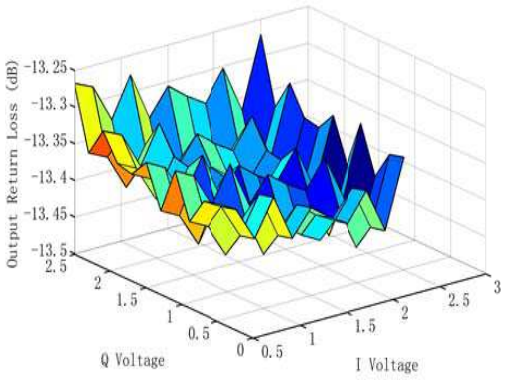

Figure 8: Output return loss vs I voltage and Q voltage.

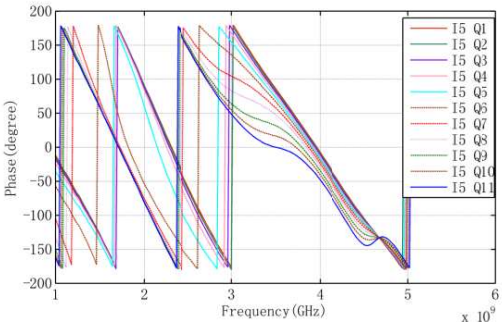

Figure 9: Phase vs Frequency and Q voltage values at 2.5v of I voltage.

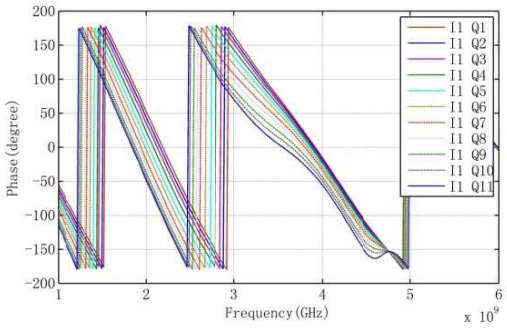

Figure 10: Phase vs Frequency and Q voltage values values at 0.5v of I voltage.

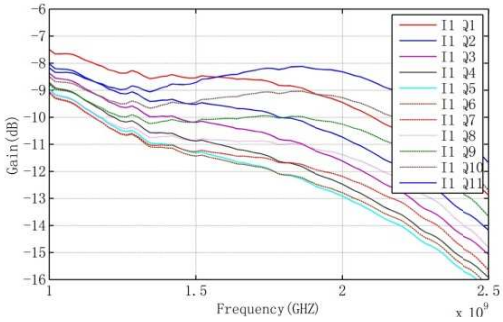

Figure 11: Frequency vs Gain and different Q voltage values under the I voltage value is 0.5 V.

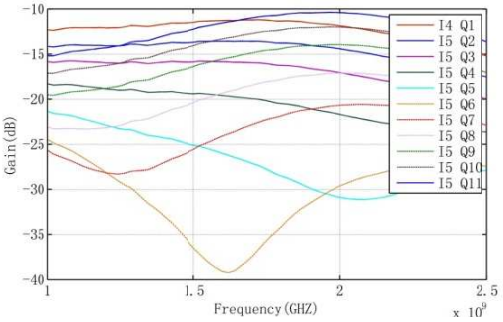

Figure 12: Frequency vs Gain and different Q voltage values under the I voltage is 2.5 V.

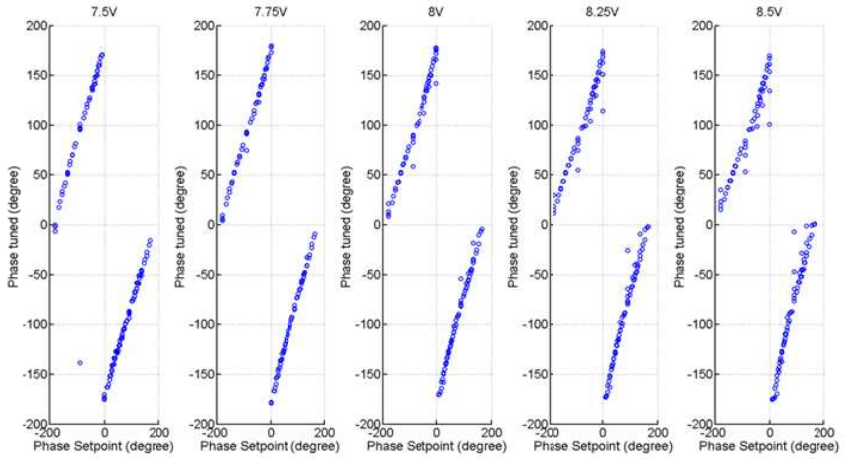

Figure 13: Phase setting vs phase and DC supply @$F = 2$ GHz.

voltage supply from 0 GHz to 6 GHz. The total number of points is 605.

All the bias voltages and I/Q supply voltages of vector modulators are programmed by control computer. At the same time, control computer reads the measured S parameters by VNA. Finally, for all the measurements of the HMC500LP3, the loss of the Balun, which is used to drive the input port, is de-embedded from these measurements. After completing the measurements, the module should be returned to the initial state and closed.

4. THE RESULT OF THE TEST

As Figure 5 and Figure 6 show, the HMC500LP3 can be used to continuously change the phase and amplitude of RF signals by up to 360 degrees and realize a range of -9 dB–(-41 dB) for the amplitude under the different voltage values of the I and Q.

Figure 7 and Figure 8 illustrate the input return loss and output return loss performance of the

different I/Q voltage values. The HMC500LP3 can achieve the input return loss greater than 17 dB and the output return loss greater than 15 dB over a broad frequency range. The chip modulator has excellent input and output matching performance.

As is shown in the Figure 9 and Figure 10, a linear correlation is found between the phase shifting degree and frequency. What is more, the slope of the lines is constant no matter what I voltage and Q voltage are. The chip model shows excellent phase linearity for various I and Q voltage values. Different I and Q voltage values can get different initial phases.

Figure 11 and Figure 12 show the Gain vs Frequency under the different I voltage values at the operating frequency. The gain flatness at 0.5 V of I voltage is much better than that at 2.5 V from 1.8 to 2.2 GHz.

Figure 13 illustrates excellent linear performance of phase setting for various DC supply. Any phase can be achieved through the vector modulator.

5. CONCLUSION

In this paper, the HMC500LP3 chip is introduced and applied into vector modulator. The outstanding measured results show that vector modulator can cover a phase shifting of 360° and are able to provide gain over 40 dB. This chip can be applied to realize active phased array antenna. Incident wave phase difference through phased array antenna is associated with the frequency and the incident angle. Given the good linear correlation between the phase shifting degree and frequency. By HMC500LP3 chip phase difference of incident wave can be compensated with a certain range.

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