A High Precision and Externally Synchronous CMOS Relaxation Oscillator

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Abstract— A high precision and externally synchronous relaxation oscillator with simple structure is proposed in this paper. The oscillator consists of the current circuits, a capacitor, two comparators, a RS flip-flop and other components. In the current circuits positive and negative temperature coefficient currents are obtained. With the current temperature compensation, a low temperature current is used to charge and discharge the capacity. By optimizing the delay of the comparators the oscillator has a good ability of control linearity In this method a high precision oscillator is obtained. Based on 0.5 µm OKI technology library, HSPICE and Cadence software is used to circuit simulation the simulation results show that the oscillator has stable output frequency and external synchronization. Under the environment of typical applications in the chip system, the frequency of the oscillation is 500.1 kHz, With the power supply temperature changing from −40°C to 125°C, the frequency migration ranges from −0.3% to +1.3%.

1. INTRODUCTION

With the advantages of light weight, small size and high efficiency, switching power supply is being widely used in almost all electronic devices. It has become an indispensable part in the development of the information industry. As a member of switching power supply with PWM circuit, the clock generation of DC/DC convertor plays a key role, its main types are: relaxation oscillator, ring oscillator and LC oscillator. Especially, the relaxation oscillator is used in capacitive sensors and monolithic power integrated circuits. A well-designed relaxation oscillator should have following features: good stability, wide frequency range and good control linearity. In this paper with the current temperature compensation, a low temperature current is used to charge and discharge the capacity, and a high-precision clock signal can then be obtained. By optimizing the delay of the comparators, the oscillator gets a good ability of control linearity. Meanwhile, in order to make the system with an oscillator works synchronously, this relaxation oscillator has a function of synchronized by external sync clock signal.

2. ARCHITECTURE OF RELAXATION OSCILLATOR

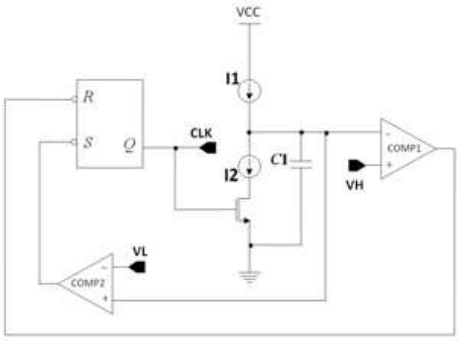

Figure 1: Layout of the tunable dual-band bandpass filter.

By taking advantage of the bi-stable characteristic of switching elements such as the flip-flop and comparator, the current circuits take turns to charge or discharge the clock capacitor. With the voltage waveform of the capacitor rising or falling, the node R and S are triggered and the state of the circuit is changed periodically. In Fig. 1, COMP1 and COMP2 are window comparators, their flipping threshold are V_H andV_L respectively.

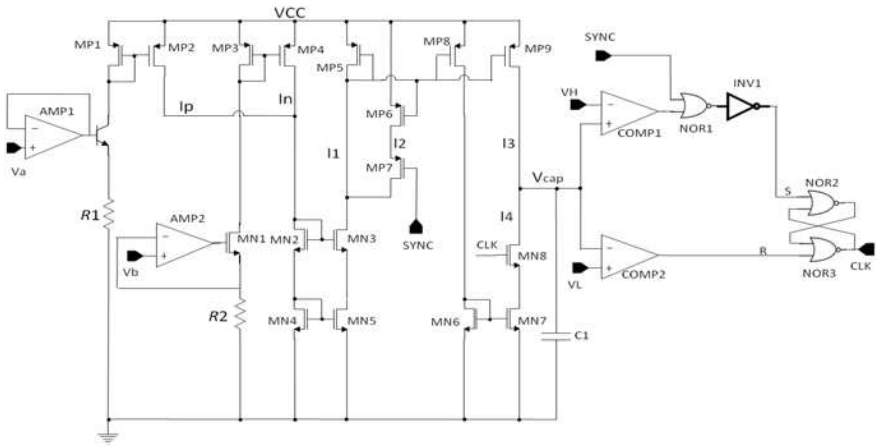

Figure 2: Layout of the tunable dual-band bandpass filter.

2.1. The Design of Relaxation Oscillator

The design of the relaxation oscillator is shown in Fig. 2, through two current circuits a temperature-compensated current is obtained. With the help of current mirror, the discharged current I_4 is greater than the charged current I_3, the capacitor voltage is toothed with frequency stability, CLK is the clock signal.

The high level V_H of the amplitude control circuit is detected by the comparator COMP1, the low level is detected by the comparator COMP2. The generation of clock is shown in Fig. 3, $tp1$ and $tp2$ are the delays produced by the two comparators. In order to reduce the frequency distortion in frequency modulator caused by non-linearity, the delay should be as small as possible. How to reduce the delay will be described in next part.

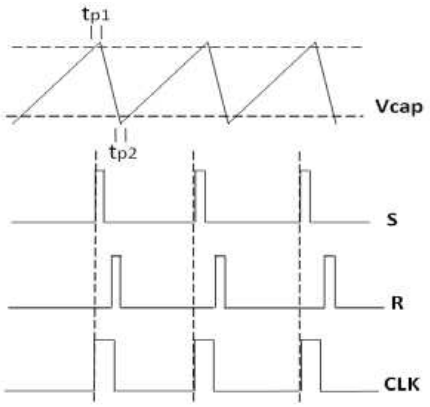

Figure 3: Sawtooth wave and generation of clock signal.

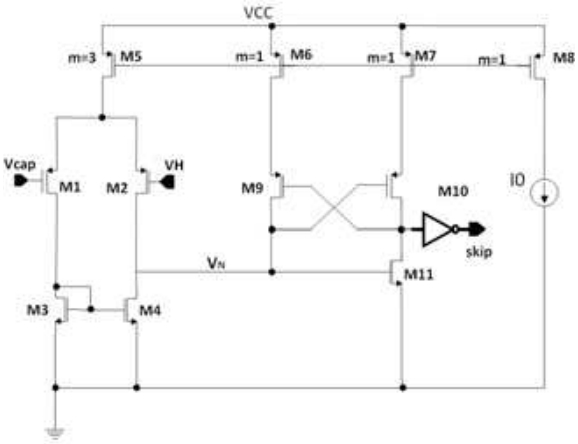

Figure 4: The comparator circuit.

The current I_p and I_n are obtained by the follower (AMP1, AMP2) tracking the reference voltage V_a and V_b respectively, which can be expressed as:

$$I_p = \frac{V_a - V_{be}}{R1} \times \frac{MP2}{MP1} \tag{1}$$

$$I_n = \frac{V_b}{R2} \times \frac{MP4}{MP3} \tag{2}$$

where $MP1$, $MP2$, $MP3$, $MP4$ mean the number of the devices in parallel respectively. With increasing temperature Vbe decreases. However $R1$ and $R2$ are resistances with positive temperature coefficient. It can be derived that I_p is the current with positive temperature coefficient and In on the contrary is the current with negative temperature coefficient. The two currents gather

to charge and discharge the clock capacitor. Through temperature compensation a high-precision clock is obtained.

2.2. The Design of the Comparator

As the RS flip-flop is triggered by the rising edge, we should reduce the delay $tp1$. The comparator circuit is designed shown as Fig. 4.

When skip signal is high and V_{cap} is higher than V_H, M9 is on and M10 is off. The drain current of M6 (I_{D6}) and that of M2 (I_{D2}) flow in M4 together. It can be derived that the drain current of M4 is larger than that of M3 and V_N is then larger than threshold voltage of M11 to keep the skip signal high. Drain current of M4 (I_{D4}) can be given by

$$I_{\mathrm{D4}} = I_{\mathrm{D2}} + I_{\mathrm{D6}} \tag{3}$$

While V_{cap} increase (V_H fixed), I_{D2} and I_{D3} decreases, V_N rises and

$$I_{\mathrm{D4}} \geq I_{\mathrm{D3}} \tag{4}$$

So the threshold of skip signal rising is achieved when I_{D4} equals to I_{D3}. As M1 and M2 work in saturation area, I_{D3} and I_{D2} can be expressed by

$$I_{\mathrm{D3}} = I_{\mathrm{D1}} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_P - V_{cap} - |V_{TP}|)^2 \tag{5}$$

$$I_{\mathrm{D2}} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_P - V_H - |V_{TP}|)^2 \tag{6}$$

Where μ_p, C_{ox}, V_{TP} and W/L stand for effective channel mobility, gate oxide capacitance per unit area, threshold voltage and wide to length ratio of PMOS. From (3), (4), (5), the condition of rising threshold can be expressed by

$$I_{\mathrm{D1}} = I_{\mathrm{D2}} + I_{\mathrm{D6}} \tag{7}$$

In Fig. 4, other current of transistors can be expressed as follow:

$$I_{\mathrm{D1}} + I_{\mathrm{D2}} = I_{\mathrm{D5}} \tag{8}$$

$$I_{\mathrm{D5}} = 3I_{\mathrm{D8}} = 3I_0 \tag{9}$$

$$I_{\mathrm{D6}} = I_{\mathrm{D8}} = I_0 \tag{10}$$

where I_0 is current bias. From (7), (8), (9) and (10), I_{D1} and I_{D2} can be expressed by

$$I_{\mathrm{D1}} = \frac{1}{2}(I_{\mathrm{D5}} + I_{\mathrm{D6}}) = 2I_0 \tag{11}$$

$$I_{\mathrm{D2}} = \frac{1}{2}(I_{\mathrm{D5}} - I_{\mathrm{D6}}) = I_0 \tag{12}$$

From (5) and (11), (6) and (12), V_C and V_P can be expressed by

$$V_P = V_{cap} + |V_{TP}| + \sqrt{\frac{2I_0}{\mu_p C_{ox} W/L}} \tag{13}$$

$$V_P = V_H + |V_{TP}| + 2\sqrt{\frac{I_0}{\mu_p C_{ox} W/L}} \tag{14}$$

From (13) and (14), the threshold voltage of skip signal rising can be given by

$$V_{cap} = V_H + \left(\sqrt{2} - 2\right)\sqrt{\frac{I_0}{\mu_p C_{ox} W/L}} \tag{15}$$

From (15), it is clear that the rising threshold voltage is lower than V_H and in this way $tp1$ can be reduced.

3. EXTERNAL SYNCHRONIZATION APPLICATION

In order to make the whole system works in unified clock synchronously, the oscillator is with externally synchronous function. The external clock signal often has an unfixed duty cycle. Such waveform is generally not conducive to an edge-triggered RS flip-flop to flip quickly, so a shaping circuit is usually needed, it may adjust the duty cycle of the external clock signal to less than 10%. This circuit is simple and is not included in our paper. When the external synchronizing signal SYNC arrives the MP7 of Fig. 2 works, and I_2 takes parts of current I_1, thus the charge-discharge current can be reduced in whole clock period. As V_{cap} is always lower than the voltage V_H, COMP1 will not overturn. The synchronous signal SYNC can be introduced through the logic gate NOR1, in this way the oscillator can work with the outside synchronous clock frequency.

4. SIMULATION RESULT

The relaxation oscillator has been implemented with a standard 0.5 µm OKI process. Our design has been simulated in a temperature ranging from −40°C to 125°C on HSPICE. The results show that the oscillator is in high precision. Table 1 summarizes the simulation result of the oscillator in different temperature.

T/°C	f_{osc}/MHz	offset/%
−40	506.5 kHz	+1.3
25	500.1 kHz	+0.02
40	504 kHz	+0.8
60	506.3 kHz	+1.26
85	499.3 kHz	−0.15
125	501.9 kHz	+0.38

Table 1: Frequency vs temperature.

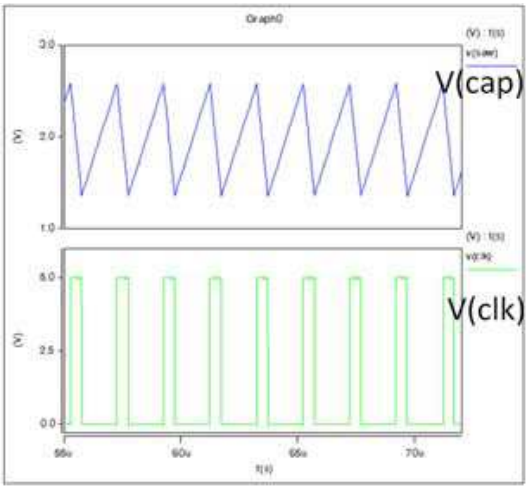

Figure 5: Simulation results of V_{cap} and OSC.

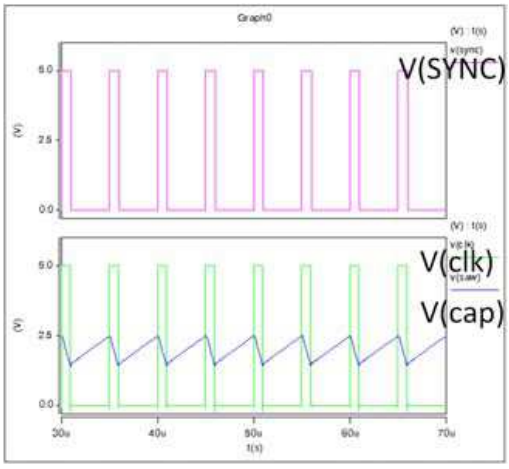

Figure 6: External synchronization with 200 kHz.

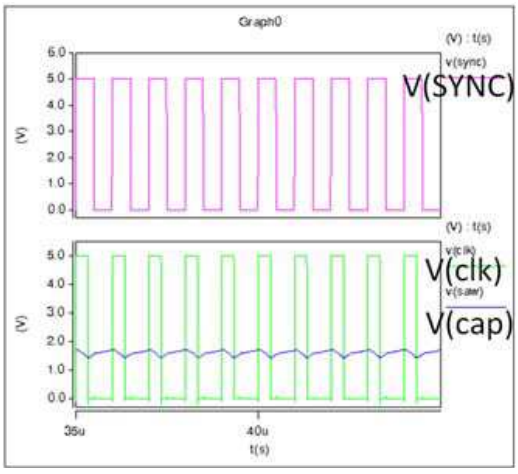

Figure 7: External synchronization with 1 MHz.

5. CONCLUSION

A high precision and externally synchronous relaxation oscillator is proposed. With the current temperature compensation, a low temperature current is used to charge and discharge the capacity.

The relaxation oscillator has been implemented with a standard 0.5 µm OKI process. This oscillator has been simulated in the temperature range of ($-40°C \sim 125°C$) on HSPICE. The results show that the oscillator is of stable frequency, high precision, and external synchronization ranging from 200 kHz to 1 MHz.

ACKNOWLEDGMENT

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