A 3–8 GHz Broadband Low Power Mixer

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Abstract—A 3–8 GHz broadband mixer is presented in this paper. This broadband mixer is low power and high conversion gain. It provides current reuse and ac-coupled folded switching. This mixer is designed in TSMC 0.18-µm CMOS technology. This broadband mixer achieves simulated conversion gain of 9 ± 1.5 dB, a single sideband noise figure lower than 15.2 dB and IIP3 better than −7 dBm. From 3–8 GHz, at supply voltage of 1.5 V power consumption without output buffer is 3.27 mW and power consumption with buffer is about 8 mW. The chip area is 1079 µm × 761 µm.

1. INTRODUCTION

In the wireless communication system, low power RF component is a trend recently. However, if we reduce the power and supply voltage, the linearity and conversion gain will be degraded. In order to accomplish low power and low voltage, holding out linearity and conversion gain without degraded is a challenge in the system. A low power mixer for UWB system input broadband matching will be a first challenge getting good return loss. Mixers executed in the receiver afford frequency translation to lower frequency or higher frequency by multiplying two signals in time domain. Mixer can be divided into two regions. One is down-conversion mixer which makes RF frequency down to IF frequency. The other is up-conversion which makes IF frequency up to RF frequency. In this work, we discuss a low power folded switch down conversion mixer.

Because of the development in the CMOS technology, we have a chance to achieve the low currents and low power in CMOS process circuit. However, it may have not enough headroom of supply voltage. Therefore, we require sufficient supply voltage to complete this mixer without cutting off transistor. A 0.3–25 GHz UWB mixer has been proposed [1], and a low voltage 2 mW 6 ∼ 10.6 GHz UWB mixer is reported in [2], a low power up-conversion mixer for 22–29 GHz UWB mixer is reported in [3], wide band and low power mixer is reported in [4].

Gilbert-based mixers can remove the undesired output LO component through the differential pairs providing opposite signal phases to cancel the feed through from the LO to the IF and generates less even-order distortion. The double-balanced mixer also has better port-to-port isolation. In traditional Gilbert cell mixers, the switching stage is stacked on the top of the transconductor stage, and resistor is stacked on the top of the switch stage. In this topology, it would compress voltage headroom. Therefore we adopt folded switching mixer. It can reduce voltage headroom of this circuit and provide broad choice of supply voltage. We can achieve the different headroom voltage from switching stage and transconductor. It will release the limit of the supply voltage. In this work as Fig. 1, we use supply voltage of 1.5 V and get good performance in this folded switching mixer.

2. ARCHITECTURE AND ANALYSIS

In Gilbert cell double-balanced mixer, nmos transistor is used as transconductor. But it may compress the headroom of the supply voltage. Then we test a resistor stacked on the top of the nmos as transconductor stage as shown in Fig. 2, the direction of signal current may be as low as possible through resistor. We would increase R to keep low ac current. However, it may limit the headroom of supply voltage. In this work, we use nmos transistor stacked of pmos transistor as transconductor, just like a CMOS inverter as Fig. 3. Because of this folded switching topology, we can achieve low supply voltage instead of limiting voltage. The components C1, L1, C2, L2, R1 are used as input matching to achieve broadband at 3.1 ∼ 8.1 GHz. M1 ∼ M4 are transconductor stage used of nmos and pmos stacking. M5 ∼ M8 are folded as switch stage. M9 ∼ M14 are used as output buffer just like a common drain with a current source.

In transconductor stage, the advantage of using pmos instead of resistor can be amplified RF signal. The pmos can be used as current reuse. It can not only supply high gain but also provide a low power. The capacitor C affords ac-coupled in RF signal and to be isolated of pmos and nmos
in DC. In RF signal, the total $g_m$ is equal to $g_{mn} + g_{mp}$ ($g_{mn}$ is the transconductance of nmos M1, and $g_{mp}$ is the transconductance of pmos). The voltage conversion gain of the mixer shown in [5]

$$CG = 20 \log \left( \frac{2}{\pi} (g_{mn} + g_{mp}) R \right)$$

Therefore, the conversion gain will be increased.

Linearity in the mixers is very important. Nonlinearity in the mixer voltage transfer function is caused by operation of the switching transistors in the linear region. The transistors in switching stage will be cutting off by the large voltage swing at the drain of the M1 and M2. Linearity almost completely decides by the input signal dynamic range. In the folded switching mixer with current reuse, the linearity can be improved by decreasing the DC drain voltages of the M1 and M2 as Fig. 1 [5].

The input matching is important in the broadband mixer. Because this mixer operates for 3–8 GHz, we can use LC ladder to match instead of transmission line. We use C1, C2, L1, L2, R1 to achieve wideband input matching. Therefore, we can achieve good performance of input return loss.
3. SIMULATION AND PERFORMANCE

The down conversion mixer is designed with 0.18\,\mu m TSMC CMOS process. Input RF frequency and LO frequency are 3–8\,GHz. Fig. 4 shows input return loss and output return loss. In 3–8 GHz, the input return loss are all lower than −10\,dB. This is good performance in broadband input matching. Fig. 5 shows LO power versus conversion gain with RF frequency at 8.1\,GHz and LO frequency at 8\,GHz. We can see about −4\,dBm of LO power, we can get the best conversion gain. With −4\,dBm of LO power, we can obtain P1\,dB with −22\,dBm as shown in Fig. 6. Simulation broadband conversion gain can be shown as Fig. 7. Broadband conversion gain are all around 9 ± 1.5\,dB. Based on two tones test with 1\,MHz offset frequency, IIP3 is −4.5\,dBm at 8\,GHz as shown in Fig. 8. For 3–8\,GHz, all IIP3 are better than −7\,dBm. Compared with other mixers in Table 1, this work provides low power, broad band, good return loss, and good performance for other section. In this mixer, power consumption is 8\,mW. Fig. 9 shows the layout of this broadband mixer. And Table 1 shows the comparison with the references.

![Figure 4: Return loss at 3 ~ 8 GHz.](image1)

![Figure 5: LO power versus conversion gain.](image2)

<table>
<thead>
<tr>
<th>Tech.</th>
<th>BW (GHz)</th>
<th>S11 (dB)</th>
<th>Conversion Gain (dB)</th>
<th>NF (SSB) (dB)</th>
<th>VDD (V)</th>
<th>Core mixer Power (mW)</th>
<th>IIP3 (dBm)</th>
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<tr>
<td>This work</td>
<td>0.18,\mu m CMOS</td>
<td>3.1–8.1</td>
<td>&lt; −12</td>
<td>7.5–10.8</td>
<td>12.4–15.2</td>
<td>1.5</td>
<td>8</td>
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<td>[1]</td>
<td>0.18,\mu m CMOS</td>
<td>0.3–25</td>
<td>&lt; −5</td>
<td>11</td>
<td>N/A</td>
<td>5</td>
<td>71</td>
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<td>[2]</td>
<td>0.18,\mu m CMOS</td>
<td>6–10.6</td>
<td>N/A</td>
<td>14 ~ 17</td>
<td>15</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>[3]</td>
<td>0.18,\mu m CMOS</td>
<td>22–29</td>
<td>&lt; −5</td>
<td>&lt; −2 ~ 0.7</td>
<td>N/A</td>
<td>1.2</td>
<td>8</td>
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<td>[4]</td>
<td>0.18,\mu m CMOS</td>
<td>0.8–2.2</td>
<td>N/A</td>
<td>10.5</td>
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<td>2.7</td>
<td>9.7</td>
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<tr>
<td>[5]</td>
<td>0.18,\mu m CMOS</td>
<td>2.4</td>
<td>N/A</td>
<td>11.9</td>
<td>13.9</td>
<td>0.7</td>
<td>3.2</td>
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<td>[5]</td>
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<td>16</td>
<td>12.9</td>
<td>1.8</td>
<td>8.1</td>
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</table>
4. CONCLUSIONS

This proposed mixer for 3 to 8 GHz with UWB system has high conversion, broad band, good return loss, moderate linearity, moderate noise figure, good isolation. This mixer is implemented in 0.18 \( \mu \)m TSMC CMOS technology. The advantages of this mixer are 10.8 dB conversion gain, lower than 11.4 dB noise figure, \(-3.4\) IIP3, and only need 3.27 mW in 3 \( \sim \) 8 GHz. It uses current reuse and folded switching to achieve low power consumption with 1.5 supply voltage. Comparing with other mixers, this mixer has the performance of low power, enough bandwidth, and good performance with current reuse.

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REFERENCES

