Cascode Feedback Amplifier Combined with Resonant Matching for UWB System

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Abstract—This paper shows the design of a broadband single-end low noise amplifier for UWB system with TSMC 0.18 \( \mu \)m CMOS processes. The proposed amplifier achieves broadband input matching by cascode feedback topology with parallel resonate cavity and the bandwidth is from 3.1 GHz to 10.1 GHz. The simulation results are as follows: 12 \( \pm \) 1 dB of gain, the input/output return loss are greater than 10 dB, minimum noise figure is about 3.3 dB, and 1 dB gain compression point is about \(-15\) dBm. The total current consumption included bias network is 9.1 mA under a 1.8 V single supply voltage. Chip area is 0.8 mm \times 0.8 mm.

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1. INTRODUCTION

The Federal Communications Commission (FCC) authorizes the unlicensed use of Ultra-Wideband (UWB) technology, this technology could be applied in various kinds of commodities. Under the FCC UWB rules, Wireless UWB has a wide bandwidth with an actual transmitting range of approximately 10 meters, and rate of transmitting data between 110 Mbps and 480 Mbps. The power dissipation needed by UWB is very low, having its frequency range at 3.1–10.6 GHz [1], and limited power emission at \(-41.3\) dBm/MHz.

As we can see apparently, UWB technology announces the coming of the high-speed wireless technology new age. This high-speed technology can be applied in wireless network, home network connection, short distance radar, etc. Specific devices like multimedia DVDs, high quality television images, satellites, and televisions are some examples of its application. Moreover, in the coming future, digital cameras, scanners, printers and MP3 players can be connected to computers wirelessly, rather than the wired connection used presently. Through the brief description of UWB technology above, we shall foresee the future prevalence of high-speed wireless consuming multimedia facilities, not to mention the immense commercial profit it will produce.

The feedback architecture is widely used in wideband amplifiers, and performs well in wideband matching and flat gain. Based on the Feedback topology, this paper shows with the combination of parallel resonate matching [2–4], using of inductance of the input matching network can be reduced and leading to smaller chip area.

The paper is organized as the following. After the introduction, comes the Section 2 describing how we design wideband LNA; the Section 3 explains the simulating result, and the last chapter is the conclusion.

Figure 1: The matching process. (a) after adding a component, \( Z_1 \) move to \( Z_2 \) and (b) \( Y_2 \) connect with parallel resonant cavity.
2. DESIGN OF AMPLIFIER

A load is placed at $Z_2$ which can be plotted on the Smith chart and it’s trace as shown in Fig. 1(a) ($\omega_2 > \omega_1$). Once we transfer $Z_2$ into admittance $Y_2(Y_2 = G_1 - jB_1$ at $\omega > \omega_0$ or $Y_2 = G_1 + jB_2$ at $\omega < \omega_0$), connect it with parallel resonate cavity, and design an appropriate resonate cavity L and C value, making resonate frequency fall on $\omega_0$, and utilizes $-jB$ offered at low frequency resonate cavity and $+jB$ offered at high frequency, $-jB_1$ and $+jB_2$ at $Y_2$ could be eliminated, as showed in Fig. 1(b), thus we achieve wideband matching. Mostly the bandwidth of the wideband amplifier does not always go through the real axis precisely, as $Z_1$ in Fig. 1(a) or make the central point of the bandwidth falls accurately on the real axis. We can move the frequency load to the real axis by adding a “component” to it.

\[
C_M = C_2 (1 - A_\nu) \quad (1)
\]
\[
R_M = \frac{R_1}{1 - A_\nu} \quad (2)
\]

Figure 2 is the LNA topology we designed. The first step is to choose the size of transistor M3 in order to achieve minimal noise figure. In next step, we decide the device value of the input matching network which is composed of L1, $C_M$, $R_M$ and L3.

$A_\nu$ is the open loop voltage gain of the LNA [5], while C2 can resist the output stage current from Cascode [6] and achieve optimization of transistor (M3) bias and increase the gm value by separating the first stage output DC level from the first stage input DC level. By doing so, power dissipation is decreased and the gain of the amplifier is increased. Also, appropriate regulation of R1 can enable the input resistance to approach the matching to 50 $\Omega$.

Figure 4 is the LNA topology we designed. The first step is to choose the size of transistor M3 in order to achieve minimal noise figure. In next step, we decide the device value of the input matching network which is composed of L1, $C_M$, $R_M$ and L3.

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![Figure 2](image2.png)  
![Figure 3](image3.png)  
![Figure 4](image4.png)  
![Figure 5](image5.png)

(a) (b)  

Figure 2: Proposed wideband amplifier.  
Figure 3: Small-Signal equivalent circuit at the input.  
Figure 4: Input matching network (a) without L3 and (b) with L3.  
Figure 5: Output stage circuit.
Figure 6: Simulation results of the proposed LNA. (a) gain, (b) noise figure, (c) input matching (S11), (d) output matching (S22), (e) stability factor.

L1 and $C_M$ will cause parallel resonate by using the inductive reactance and capacitive reactance appeared before and after the resonating, we can eliminate the reactance of the circuit we want to match. Then, the impedance in certain frequency range will approach 50 $\Omega$; thus the broadband matching achieved. Inductor L3 can move the matching bandwidth to the real axis. As showed in Figs. 4(a) and (b), we find that the closer the high frequency approaches the central of the circle, the better matching effect achieves. With better matching effects, the gain will improve without extra power dissipation.

There is an amplifying effect at the output stage also, which can increase the total gain. As we can see in Fig. 5, by using active load, the output impedance equals $R_{\text{out}} = 1/g_{m3}/r_o \approx 1/g_{m3}$. Then, regulate $1/g_{m3}$ as approximately 50 $\Omega$, and we achieve matching at the output.

In order to extend the Bandwidth, the output load of cascode amplifier will be done with inductive-peaking technique as showed in Fig. 2. Inductor L2 will give the cascode amplifier output an extra zero to eliminate the pole, and extend the bandwidth. Because the Cascode stage is the main amplifier, the current being nearly 6 mA, we will parallel 6–7 resistors to prevent the wire be broken in actual application. Knowing that process variations usually occur in semiconductor process, this circuit adopts PMOS to complete the resister device of inductive-peaking. When operating PMOS at the deep triode region [7], the MOS device performs like a resistor (see M1 in Fig. 2), keeping the gate voltage of M1 low, so that all loads of the voltage output amplitudes remain in the deep triode region. Resistance $R_{\text{on}}$ is showed in Equation (3).

$$R_{\text{on}} = \frac{1}{\mu_p C_{\text{ox}} \left( \frac{W}{L} \right) (V_{DD} - V_b - |V_{THP}|)}$$ (3)
3. SIMULATION RESULTS

The proposed architecture shown in Fig. 2 is applied to a 3.1~10.1 GHz broadband amplifier based on 0.18 µm CMOS technology. The simulated maximum gain is 13.1 dB at 6.6 GHz and 1 dB of gain flatness as shown in Fig. 6(a). The simulated NF shows a minimum value of 3.3 dB at 8.9 GHz as shown in Fig. 6(b). The input/output matching simulation results are shown in Figs. 6(c) and (d) respectively. S11 and S22 of LNA are less than $-10$ dB in the frequency ranges of interest. The stability of LNA was simulated as shown in Fig. 6(e), and it is satisfied in the operation frequency range. The input third intercept point is performed at 5.5 GHz and 10.5 GHz. The performance simulation results for proposed LNA are summarized in Table 1.

Table 1: Simulation results of wideband LNA.

<table>
<thead>
<tr>
<th>Process</th>
<th>TSMC 0.18 µm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth (GHz)</td>
<td>3.1~10.1</td>
</tr>
<tr>
<td>S11 (dB)</td>
<td>&gt; 10 dB</td>
</tr>
<tr>
<td>S21 (dB)</td>
<td>12 ± 1</td>
</tr>
<tr>
<td>S12 (dB)</td>
<td>&gt; 30 dB</td>
</tr>
<tr>
<td>S22 (dB)</td>
<td>&gt; 10 dB</td>
</tr>
<tr>
<td>NF (dB)</td>
<td>3.3 ~ 5</td>
</tr>
<tr>
<td>P1dB (dBm)</td>
<td>$-15.7$ @ 5.5 GHz</td>
</tr>
<tr>
<td></td>
<td>$-9$ @ 10.5 GHz</td>
</tr>
<tr>
<td>IIP3 (dBm)</td>
<td>$-6.6$ @ 5.5 GHz</td>
</tr>
<tr>
<td></td>
<td>$-1.7$ @ 10.5 GHz</td>
</tr>
<tr>
<td>Power Consumption (mW)</td>
<td>16.4</td>
</tr>
<tr>
<td>Chip Size (mm×mm)</td>
<td>0.8 × 0.8</td>
</tr>
</tbody>
</table>

4. CONCLUSIONS

The novel broadband amplifier is achieved by combining the cascode feedback topology and parallel resonant cavity. The designed LNA is applied to a 3.1 ~ 10.1 GHz UWB amplifier implementation based on 0.18 µm CMOS technology. The simulation results show 12 dB gain, minimum noise figure 3.3 dB, and less than $-10$ dB input/output matching within bandwidth with 16.4 mW power consumption. This proposed broadband LNA could be used for UWB system.

REFERENCES